

CVD COATED COPPER SUBSTRATE SRF CAVITY RESEARCH AT CORNELL UNIVERSITY*

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Abstract

Chemical vapor deposition (CVD) is a promising alternative to conventional sputter techniques for coating copper substrate cavities with high-quality superconducting films. Through multiple SRF-related DOE SBIR awards, Ultramet has developed CVD processes and CVD reactor designs for SRF cavities, and Cornell University has conducted extensive RF testing of CVD coated surfaces. Here we report results from thin-film CVD Nb₃Sn coated copper test plates, and for thick-film CVD niobium on copper, including full-scale single cell 1.3 GHz copper substrate cavities. Detailed optical inspection and surface characterization show high-quality and well-adhered coatings. No copper contamination is found. The Nb₃Sn coated plates have a uniform Nb₃Sn coating with a slightly low tin concentration (19 -22%), but a BCS resistance well in agreement with predictions. The CVD Nb coatings on copper plates demonstrate excellent adhesion characteristics and exceeded surface fields of 25 mT without showing signs of a strong Q-slope that is frequently observed in sputtered Nb cavities. Multiple single-cell 1.3 GHz copper cavities have been coated to date at Ultramet, and results from RF testing of these are presented and discussed.

INTRODUCTION

Superconducting radio frequency (SRF) cavities are a key component for modern accelerators. Bulk niobium has been widely used in SRF cavity fabrication. The performance of the bulk Nb cavities achieved high quality factor and high gradient. Since high RRR Nb is quite expensive, thin-film Nb has been employed for low-frequency and high-beta SRF cavities to save material cost. More than three hundred 350MHz and sixteen 400MHz Nb-Cu thin-film cavities were installed and operated in LEP II and LHC respectively [1]. As the quality of the Nb layer has been improved, thin-film Nb is becoming an option that can be applied to high-frequency (> 500MHz) SRF cavities. In addition, the Nb-Cu cavities have higher thermal stability because the thermal conductivity of copper (~300-2000 W/(m·K)) is much larger than that of Nb (~75 W/(m·K)). Another advantage of a thin film is that the Nb layer can be uniformly coated on complex shaped parts absent machining defects on surface.

* Work supported by U.S. DOE SBIR phase-II award DE-SC0015727.

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CHEMICAL VAPOUR DEPOSITION

The conventional method of coating thin-film Nb layers is via sputtering techniques. One of the main limitations of the sputtered SRF cavities is Q-slope, as is described in Refs [2, 3]. Another drawback of the sputtering is that the Nb layer can have poor adhesion to the copper substrate. It had been observed that the Nb layer of some sputtered Nb-Cu cavities peeled off during a standard high-pressure water rinsing (HPR) [4].

As an alternative method, chemical vapor deposition can coat a high-quality Nb or Nb₃Sn layer on a copper substrate with complex shaped structure. In the CVD process one or more precursors and reactant gasses are exposed to the substrate (in a chamber called the reactor) and either react or decompose, leaving behind the coating material. A common process for coating niobium is to vaporize NbCl₅ (the precursor) in a bubbler, carry it into the reactor using a gas e.g. argon, while simultaneously pumping in hydrogen gas (the reactant gas). The reaction $2 \text{NbCl}_5 + 5 \text{H}_2 \rightarrow 2 \text{Nb} + 10 \text{HCl}$ takes place, leaving niobium on the substrate while the remaining gasses being pumped out of the reactor. In addition, the substrate is heated e.g. to 700 °C, so that the reaction primarily takes place on the substrate [5-8].

CVD can form a metallurgical diffusion bond layer on a substrate surface, which is strong enough to withstand high-pressure water rinsing (HPR). In addition, the strong bonding promotes good thermal contact minimizing thermal resistance across the Nb-Cu interface. CVD has a high deposition rate of ~300um/hour, allowing to make both thick and thin films of highly pure Nb. Potentially, impurities can be introduced in the CVD Nb layer to increase Q₀ via impurity doping.

To fully optimize CVD for SRF cavities, several technical and performance challenges must be overcome. The CVD Nb must be:

1. Of high quality and purity
2. Sufficiently thick and robust to be compatible with conventionally proven surface treatments e.g. HPR, mechanical and chemical polishing, etc.;
3. Of uniform thickness over a large surface area;
4. Able to be applied to complex geometrical structures e.g. a full-scale cavity;
5. Of low residual resistance (R₀);
6. Achieve High accelerating gradients (E_{acc});
7. Not show severe Q-slope.

Ultramet researchers began developing CVD process technologies for use in SRF applications in 2005 through

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DOE-SBIR funding. A collaboration supported by the U.S. DOE SBIR program between Ultramet and Cornell University to develop CVD for SRF started in 2012. Since then, high quality CVD Nb-Cu samples have been coated at Ultramet and tested at Cornell, as is shown in Fig. 1. The RRR of the samples achieved more than 250, which was a first milestone for the CVD R&D work. In 2016, Ultramet successfully coated a 5" diameter Nb-Cu plate. A bulk CVD Nb cavity was produced successfully in 2012.



Figure 1: RRR measurement of a CVD Nb-Cu sample at Cornell showing RRR high than 250.

CVD Nb-Cu CAVITIES

1.3GHz CVD Nb on Cu Single-Cell Cavities

The 1.3GHz CVD Nb on Cu cavity work started in 2017 supported by a DOE SBIR phase-II award. To date, three CVD Nb on Cu substrate cavities (LTE1-CVD-2, -3, and -4) have been successfully coated at Ultramet, and tested at Cornell as shown in Fig. 2.

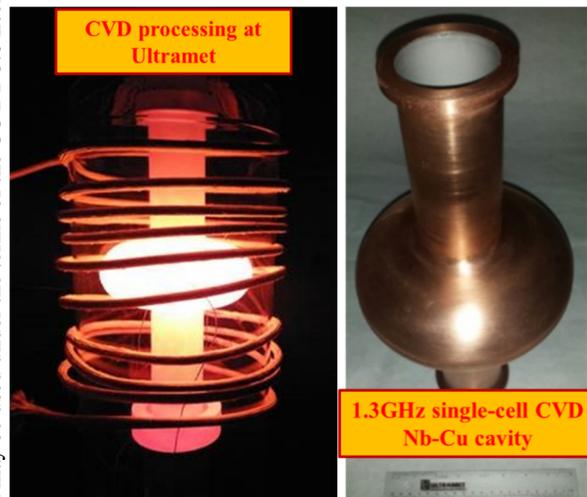


Figure 2: 1.3GHz CVD Nb-Cu SRF cavity; left plot shows CVD processing at Ultramet; right plot shows the CVD cavity.

The cross-section SEM images of a sample cut from the cavity LTE1-CVD-3 (Fig. 3) showed that the average

thickness of the Nb layer is more than 200um, thereby enabling surface treatments, e.g. electropolishing and tumbling.

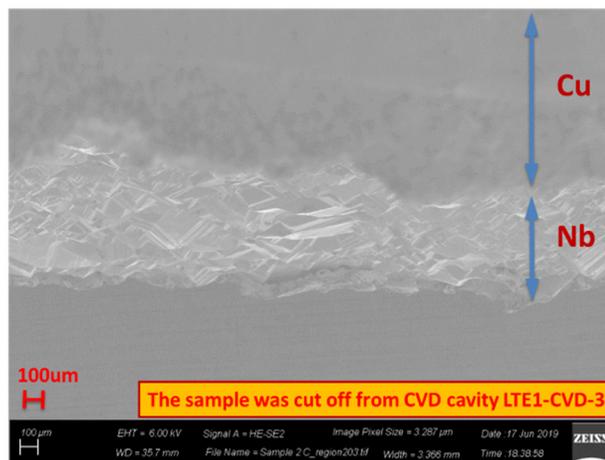


Figure 3: Cross-section SEM of a sample cut off from LTE1-CVD-3.

CVD Cavity Test Preparation at Cornell

The primary surface treatment used for the first CVD cavities tested was vertical electropolishing (Cornell VEP setup is shown in Fig. 4). LTE1-CVD-2 received 10um VEP followed by HPR and clean assembly in class 10 cleanroom in preparation for RF testing. LTE1-CVD-3 was first RF tested (Vertical Tests 1 and 2), and then received 5um VEP before additional RF testing was performed (Vertical Tests 3 - 5).

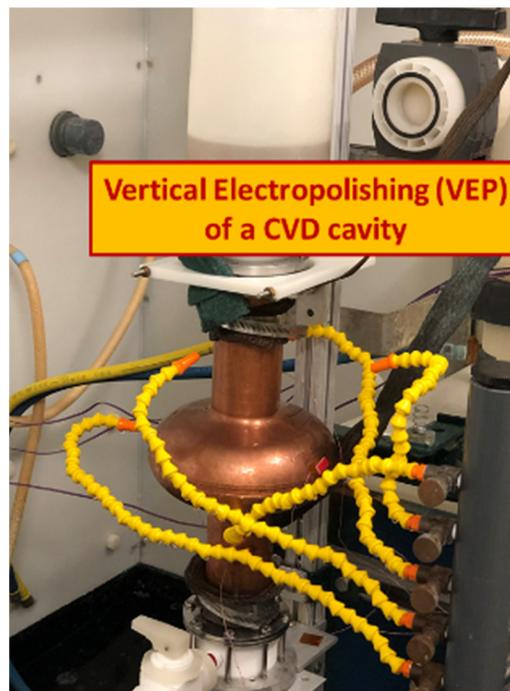


Figure 4: Vertical electropolishing (VEP) of a CVD cavity at Cornell University.

The standard vertical test (VT) setup is equipped with a Helmholtz coil for ambient magnetic field compensation, as well as a slow cool stinger for cooldown speed controlling, as is shown in Fig. 5 (left). The temperature mapping set up, shown in Fig. 5 (right) was installed for quench location detection.

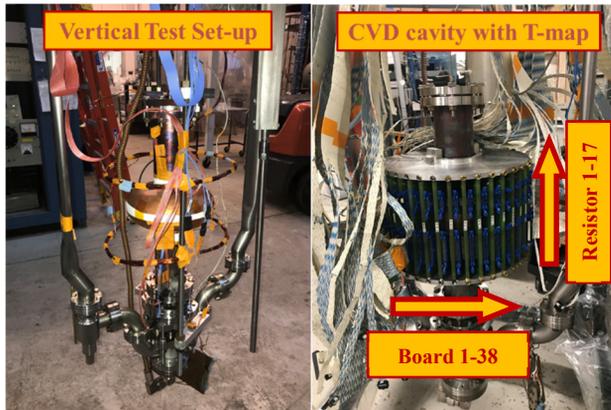


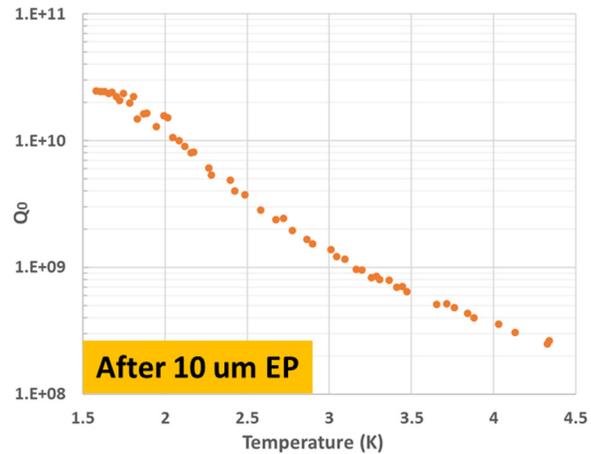
Figure 5: Vertical set-up of the CVD cavities; left plot shows Helmholtz coil from magnetic field compensation; right plot shows full temperature mapping system dressed on a CVD cavity.

CVD Cavity Test Results

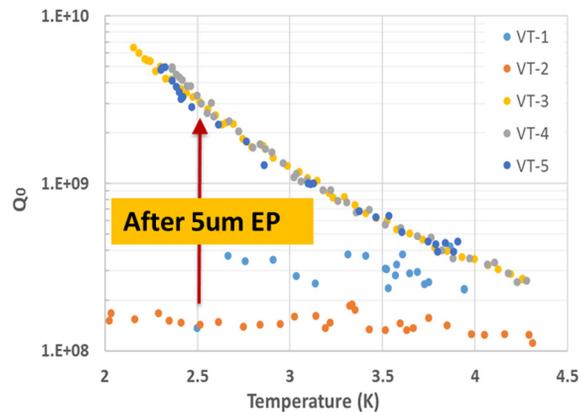
The Q_0 vs. temperature curves of LTE1-CVD-2 and 3 are shown in Figure 6 (a) and (b) respectively. The highest Q_0 of CVD-2 achieved $\sim 2.5 \times 10^{10}$ at 1.6K; the Q_0 at 2K was higher than 1×10^{10} which is quite close to the Q-value of a heavy (e.g. 100um) electropolished cavity. LTE1-CVD-3 was tested before and after the VEP for performance comparison. The Q_0 before VEP (in VT1 and 2) was dominated by high residual resistance due to contaminations on surface from CVD processing. After 5um VEP, the contamination was removed, and the Q-value was significantly improved. The high Q results indicate that the dirty surface layer from CVD is very shallow; a light surface removal can clean the surface and the surface below is pure and clean.

The mean free path (MFP) and residual resistance (R_0) are important parameters in evaluating surface purity and

cleanness, which can be obtained from frequency vs. temperature and surface resistance vs. temperature measurements. The extracted MFP and R_0 as well as other superconducting parameters of LTE1-CVD-1 and 2 are listed in Table 1. The large MFP ($\sim 1000\text{nm}$ and above) and low R_0 ($< 10\text{ n}\Omega$) of the both cavities indicate that the CVD Nb layers coated on the cavity surfaces are very pure and clean.



(a) LTE1-CVD-2 Q_0 vs. temperature curve.



(b) LTE1-CVD-3 Q_0 vs. temperature curves.

Figure 6: Q_0 vs. temperature curves of (a) LTE1-CVD-2 and (b) LTE1-CVD-3.

Table 1: Fitted Superconducting Parameters of LTE1-CVD-2 and 3

Cavity	Mean Free Path (nm)	T_c (K)	Energy Gap	R_0 (nm)
LET1-CVD-2	4500	9.20	1.994	8.5
LET1-CVD-3	948	9.21	1.910	5.4

Measuring RF dissipation from trapped flux is another powerful tool to evaluate the Nb layer purity. In LTE1-CVD-2 tests, two cooldowns were performed with ambient magnetic field ~ 150 mGauss and with the field < 10 mGauss, respectively. Since the cooldown rate was slow, it can be assumed that nearly 100% flux were trapped. The

sensitivity was found to be $0.73\text{ n}\Omega/\text{mGauss}$, calculated from R_0 vs. ambient magnetic field, as is shown in Fig. 7. The sensitivity value was close to an electropolished cavity [9], again indicating that the Nb layer coated on the cavity is pure. In summary, high purity and cleanness were demonstrated by a series of excellent measurement results,

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i.e. high- Q_0 ($> 1 \times 10^{10}$ at 2K), low R_0 (< 10 n Ω), large MFP (> 900 nm), and low flux trapping sensitivity (~ 0.73 n Ω /mGauss).

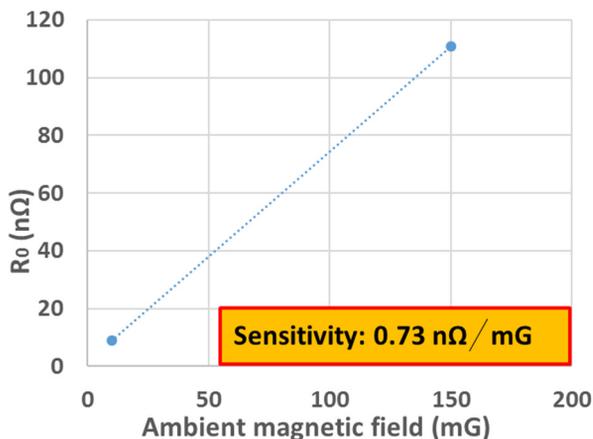


Figure 7: Flux trapping sensitivity measurement indicating that the surface of the CVD cavity is very clean.

The Q -slope comparison with a sputter cavity is shown in Fig. 8. The LET1-CVD-2 Q -value dropped by about 10%, while the Q_0 of LET1-CVD-3 dropped 20%; as a comparison, a sputtered cavity Q_0 dropped 50% [3].

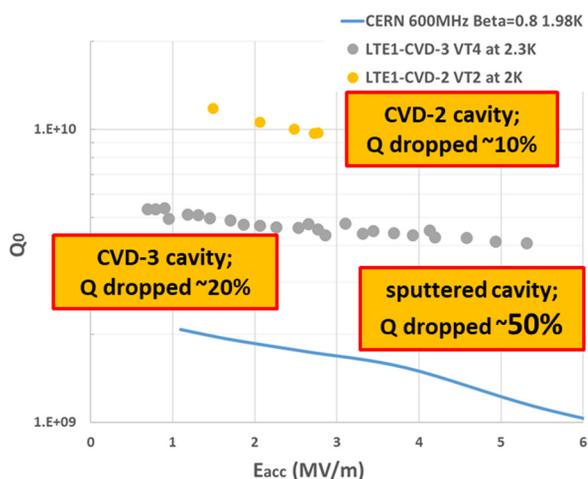


Figure 8: Q -slope comparison between the CVD cavities and a sputtered cavity [3].

The Q_0 vs. E_{acc} curves of LET1-CVD-2 and -3 of all vertical tests are plotted in Fig. 9. The temperature of the LET1-CVD-3 data taking was limited to > 2.3 K due to a cavity cold leak. The quench fields of LET1-CVD-2 and -3 were ~ 3 MV/m and ~ 5 MV/m respectively. To determine the nature of the cavity quench, in VT5 of CVD-3, a full temperature mapping system was mounted onto the cavity. The measured heating map taken at 3.28MV/m is shown in Fig. 10 (a), indicating small heating uniformly around the entire high magnetic field region of the cavity. The cavity exhibited quench over a large area, as is shown in Fig. 10 (b). This quench data indicates that the cavity did not quench at a single spot due to a surface defect. Instead,

there likely is some common feature over a large surface area that caused the quench. Motivated by this conclusion, Nb-Cu sample studies were carried out to better understand surface characteristics of the CVD coatings, as is described in the next section.

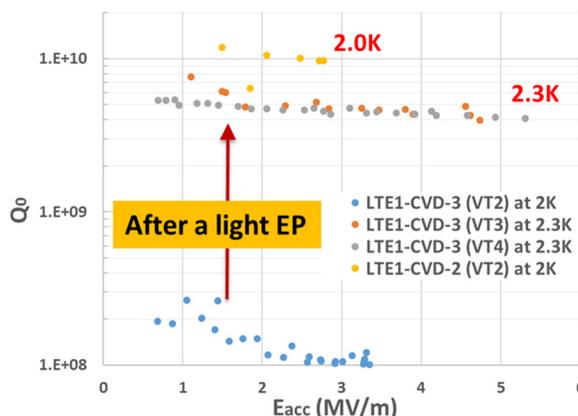
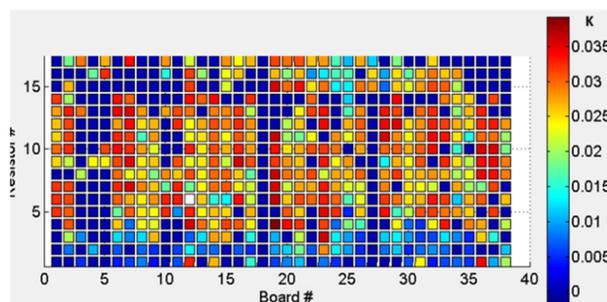
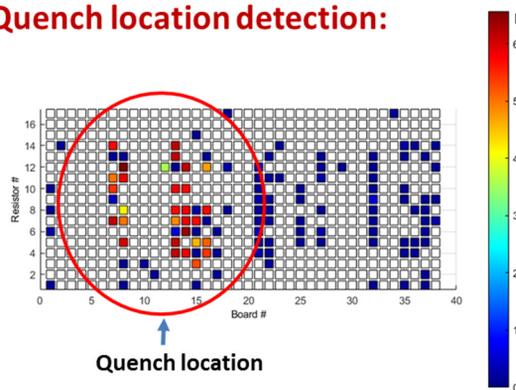


Figure 9: Summary of Q_0 vs. accelerating gradient curves for LET1-CVD-2 and -3.



(a) Temperature mapping result of LTE1-CVD-3 at $E_{acc}=3.28$ MV/m;

Quench location detection:



(b) Quench location detection showing the quench spot is large.

Figure 10: Temperature mapping results of LTE1-CVD-3.

CVD NB-CU SAMPLE STUDY

Two witness samples were coated with the cavities during the CVD processing. One sample surface was treated by 10 μ m electropolishing. SEM scan images of the non-electropolished sample and the electropolished sample are

showed in Fig 11. The non-electropolished sample exhibits sharp edges on grain boundaries; while after 10um EP, the sharp edges were significantly smoothed.

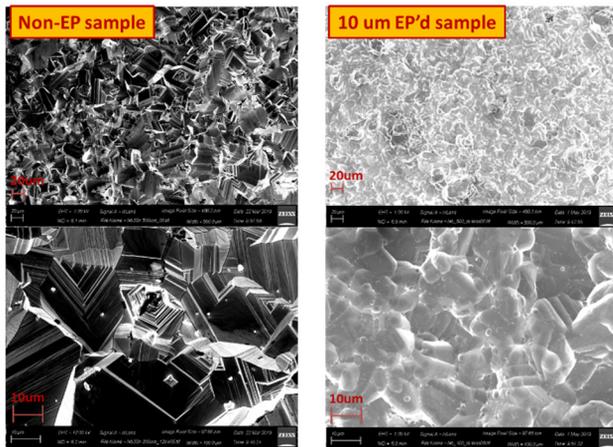


Figure 11: SEM scan comparison on electropolished and non-electropolished samples.

Cross-section SEM was carried out on the two samples to view surface topology. The comparison images are shown in Fig. 12. The images of the non-electropolished sample show significant surface roughness, with sharp-edged bumps of approximate 90um height. Similar bumps were found on the 10um electropolished sample, but with edges smoothed by the electropolishing. It has to be pointed out that the cavity surfaces appear to be smoother than these sample surfaces.

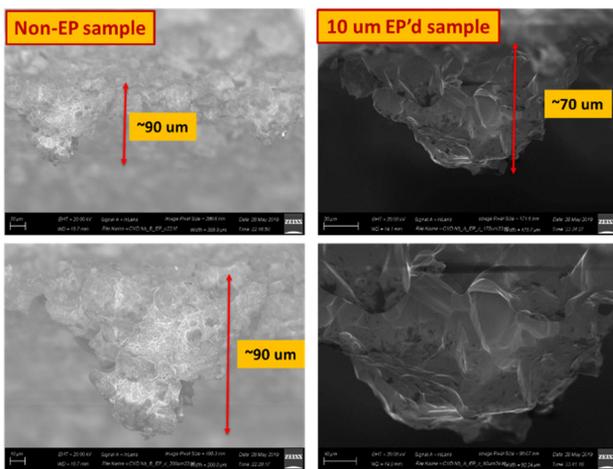


Figure 12: Cross-section SEM comparison of non-electropolished and electropolished samples.

CVD Nb₃Sn-Cu PLATES

The CVD can also be used to coat Nb₃Sn on copper substrate. A 5-inch large Nb₃Sn-Cu plated (Fig. 12 left plot) was successfully coated at Ultramet and tested via the 4GHz sample host cavity at Cornell. The SEM image in Fig. 13 (right) shows that the coating layer is uniform. The Sn content of the coating was measured to be at 19%-22%, which is a bit lower than the ideal percentage target of 25%.

This lower Sn percentage drops the critical temperature of Nb₃Sn from 18K to 6-8K [10]. Hence, the surface resistance calculated by BCS theory is increased to the uΩ level. The surface resistance measurement of the plate is close to this theoretical calculation, as is shown in Fig. 14.

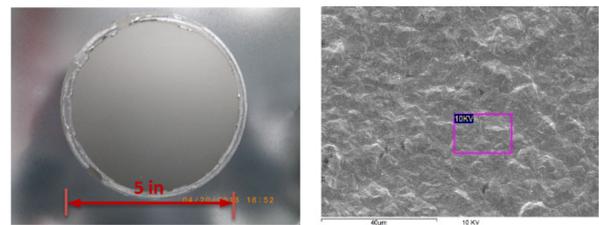


Figure 13: A 5-inch large Nb₃Sn-Cu plate coated by CVD (left plot); and SEM images (right plot) indicating that the coating layer is uniform.

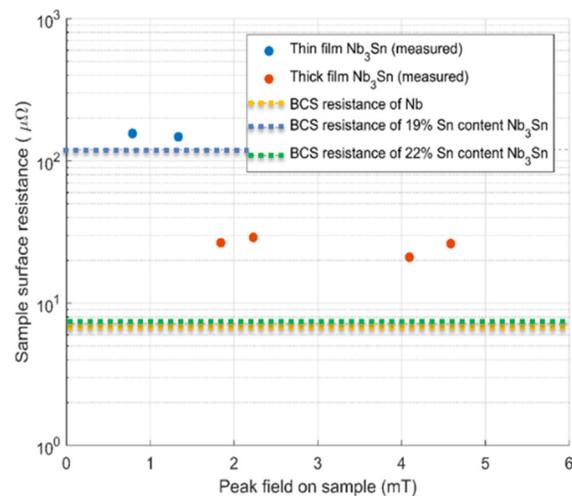


Figure 14: The surface resistance vs. magnetic field result of the Nb₃Sn-Cu plate compared with the calculation using BCS theory.

CONCLUSION

In this paper, test results are presented and discussed of demonstrated high performance of the first CVD Nb coated copper substrate SRF cavities. RF measurements show that high-purity Nb (RRR>250, MFP>900nm) was successfully coated on the cavity surfaces. The cavities reached high-Q (>1×10¹⁰ at 2K) with low residual resistance (R₀<10) after 5-10um EP. The CVD cavities show only modest Q-slope with increased RF field, much lower than seen in typical sputtered cavities. Surface roughness caused the cavities to quench around 3-5MV/m. The SEM images reveal sharp edges and 70-90um high bumps on witness samples. Future preparations will use mechanical polishing prior to electropolishing to reduce surface roughness. Excellent adhesion of the CVD niobium layer on the copper substrate was demonstrated, without layer peeled off after electropolishing, tumbling and HPR.

A first of-its-kind 5-inch diameter Nb₃Sn-Cu plate was successfully coated by CVD. The measured Sn content was 19-22% which is close to the ideal target of 25%. Surface

resistance measured is consistent with predicted values from the BCS theory calculation.

ACKNOWLEDGEMENTS

The authors would like to express their gratitude for the strong support by the U.S. DOE SBIR program through multiple SBIR awards.

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