Modern Digital Synchronization Systems for Large Particle Accelerators

Fatkin G. A.

Modern synchronization systems

Common time

Events

Timestamping

LLRF distribution

Dynamic delay compensation

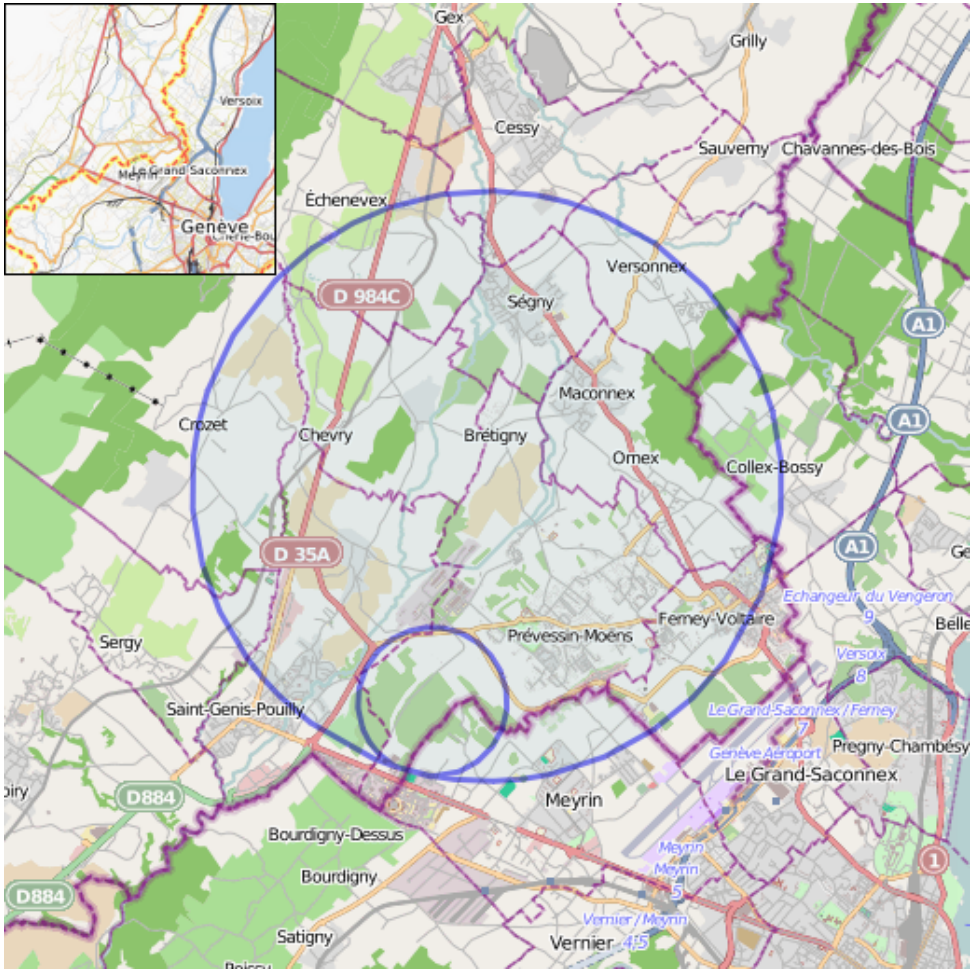
Machine Safety and Interlocks

Achievements

Synchronization precision is several ps

Distances from 100 m up to 10 km

Large number of channels » 100



White Rabbit

(CERN)

EVG и EVR

(Micro Research Finland)

Greenfield

J-PARC

BINP

Micro-Research Finland Oy

LIA 20

Frequency sources

Quartz

$5 \cdot 10^{-10}$ /day

Thermostatic quartz

$5 \cdot 10^{-11}$ /day

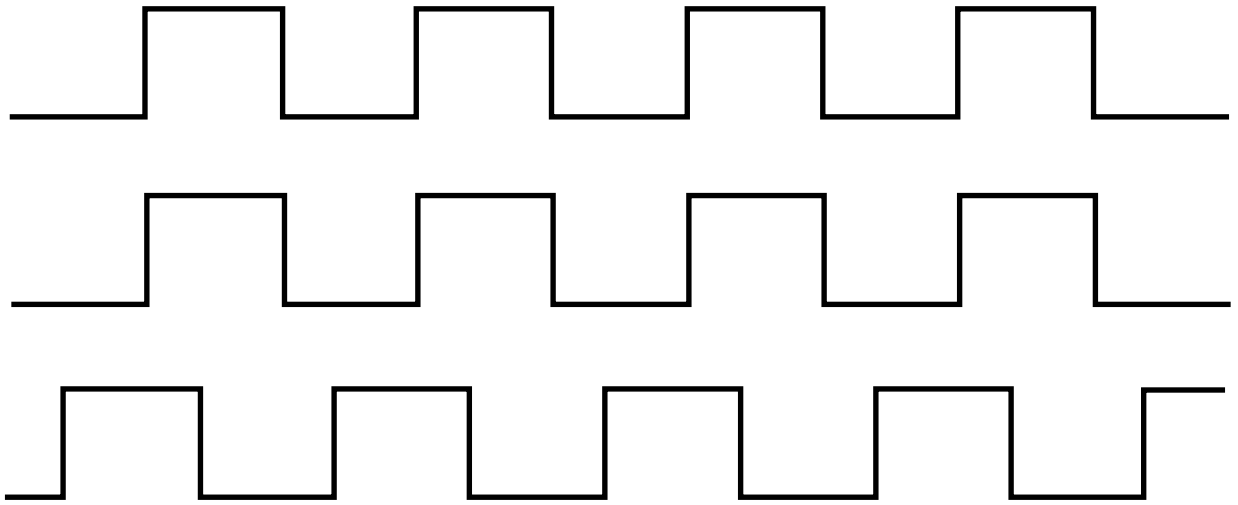
Rubidium generator

$5 \cdot 10^{-11}$ /month - $3 \cdot 10^{-10}$ /month

GPS/GLONASS (Atomic clock)

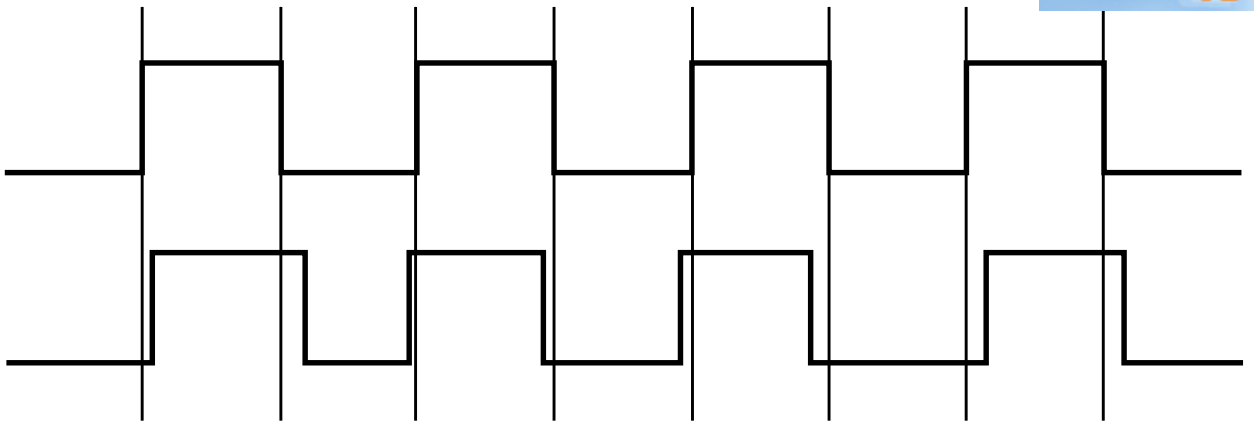
$5 \cdot 10^{-14}$ /month

Synchronisation

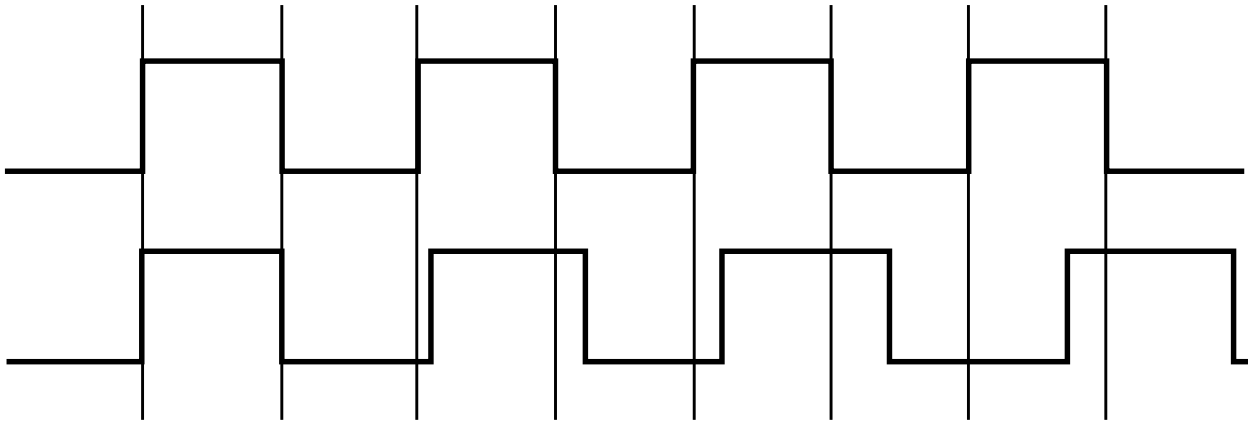


Syntonization
Phase alignment
Counter compensation

Jitter



Long-term frequency УХОД



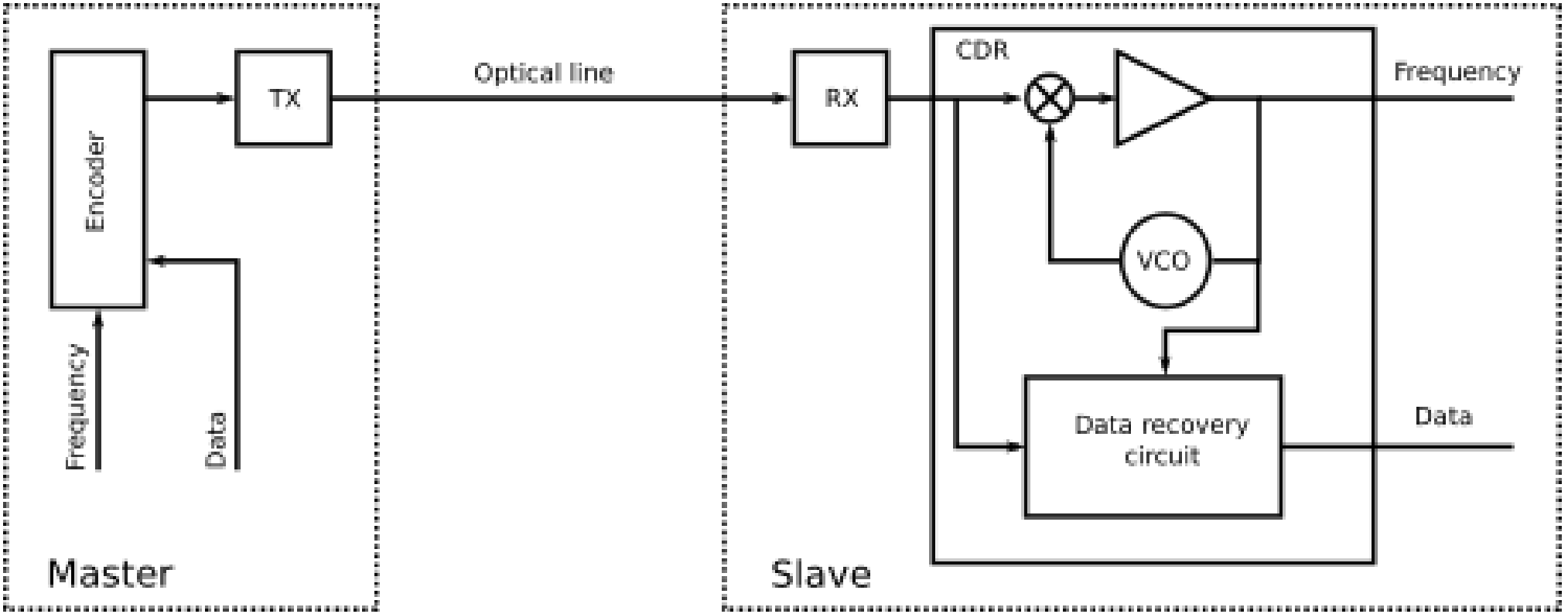
What should be done

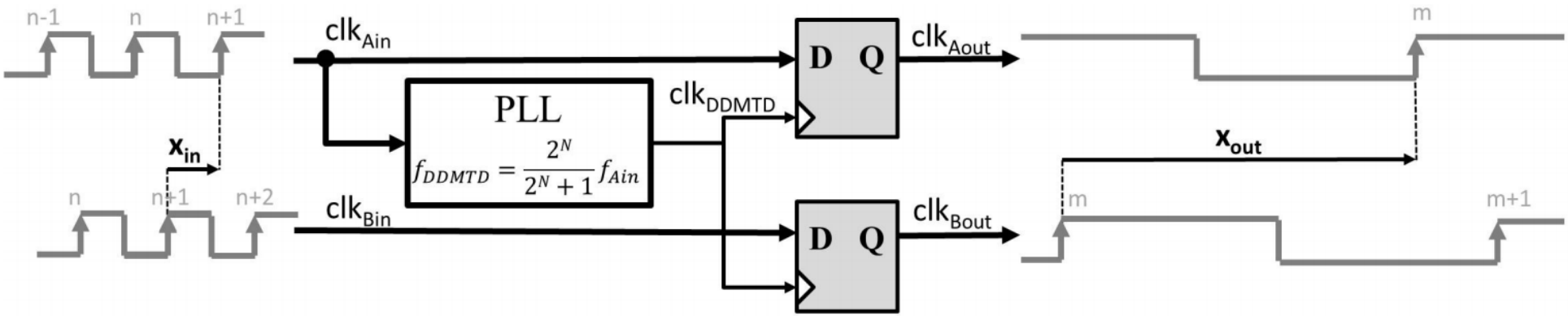
1. Frequency synchronization

2. Events transfer

3. Determination of delays and phase differences

Principle of operation





- Used for precise phase measurements
- Outputs are at much lower frequencies, easier to measure

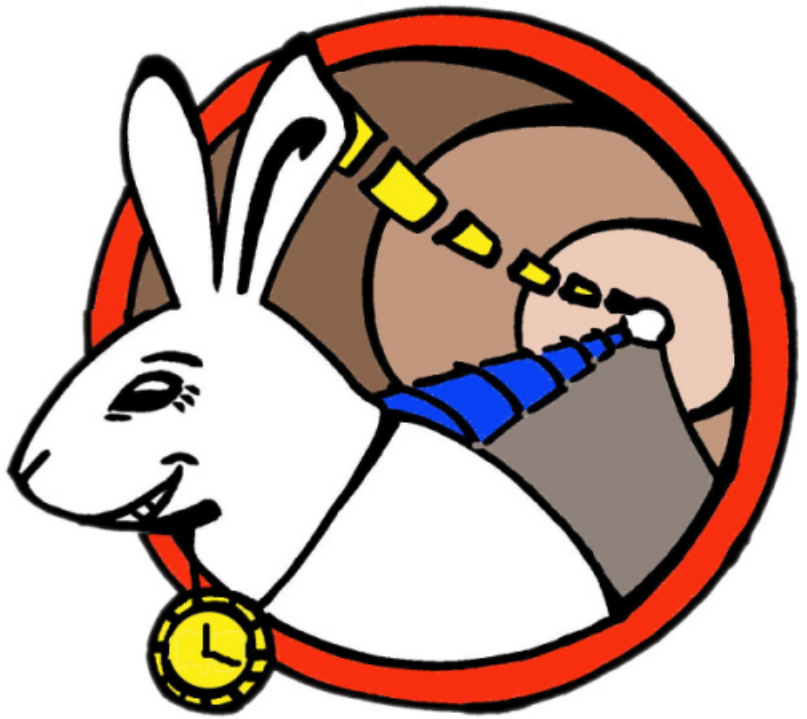
White Rabbit

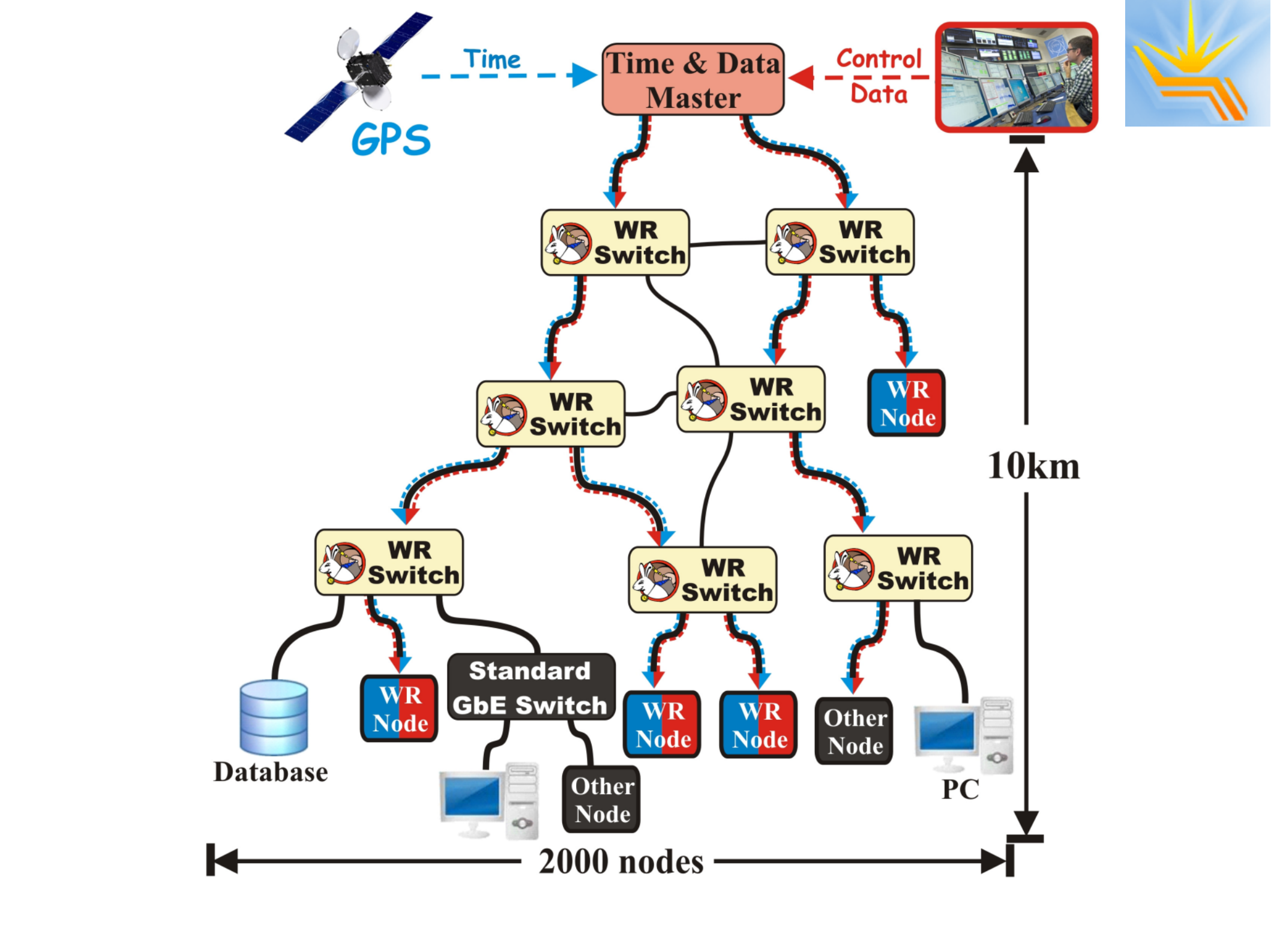
Protocol for synchronization of distributed nodes with sub-nanosecond precision (~10 ps jitter)

125 MHz clock + Ethernet messages

Open Hardware

Open Software



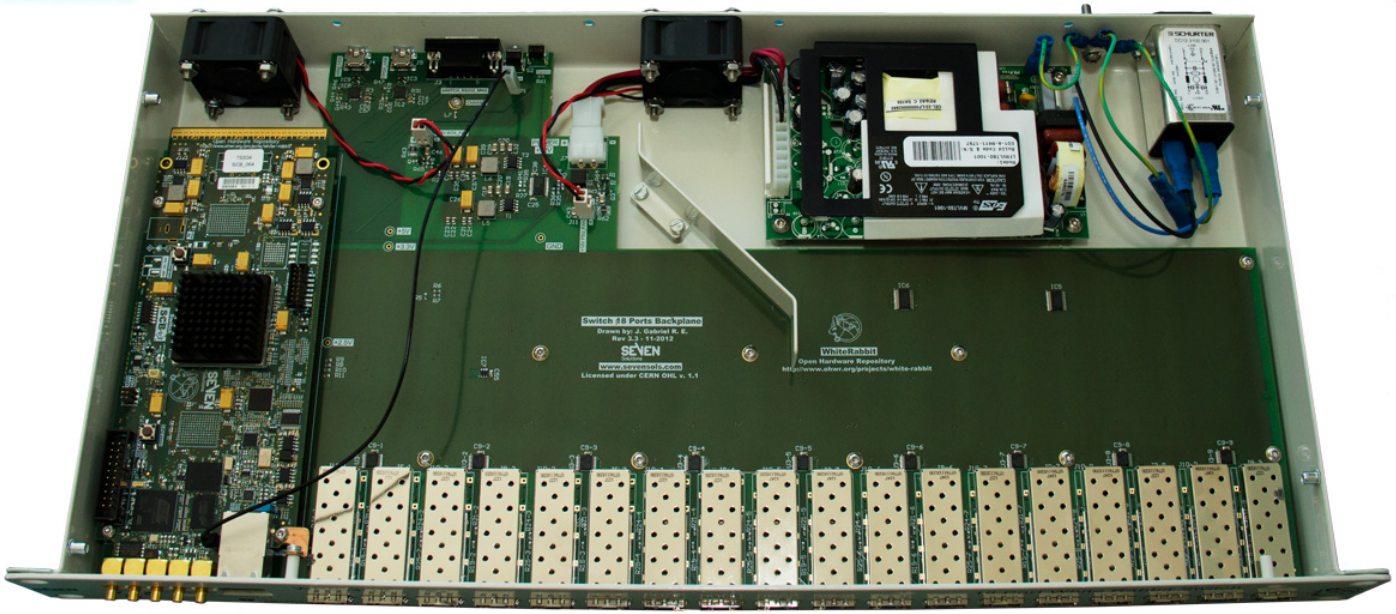

GPS
Time
Time & Data Master
Control Data
WR Switch
WR Switch
WR Switch
WR Switch
WR Node
WR Switch
WR Switch
WR Switch
Database
WR Node
Standard GbE Switch
WR Node
WR Node
Other Node
Other Node
PC
10km
2000 nodes

White Rabbit Switch

Front Panel	
Clocks I/O	5 SMC coaxial connectors: ▪ 10 MHz reference clock input (GPS/Cesium) ▪ 10MHz & 62.5 MHz output reference clock ▪ 1xPPS Input & 1xPPS Output
Ports	18 x SFP cages* **SFP transceivers are not included in all packages. Seven Solutions recommends 1.25Gbps, 1490/1310 nm, Single Fiber Bi-directional SFP.*
Management	100Base-T Ethernet (Remote) USB Mini-B (Local)

Back Panel	
GPS	RS232 Port (input from GPRMC)
Debug	USB Mini-B FGPA USB Mini-B ARM

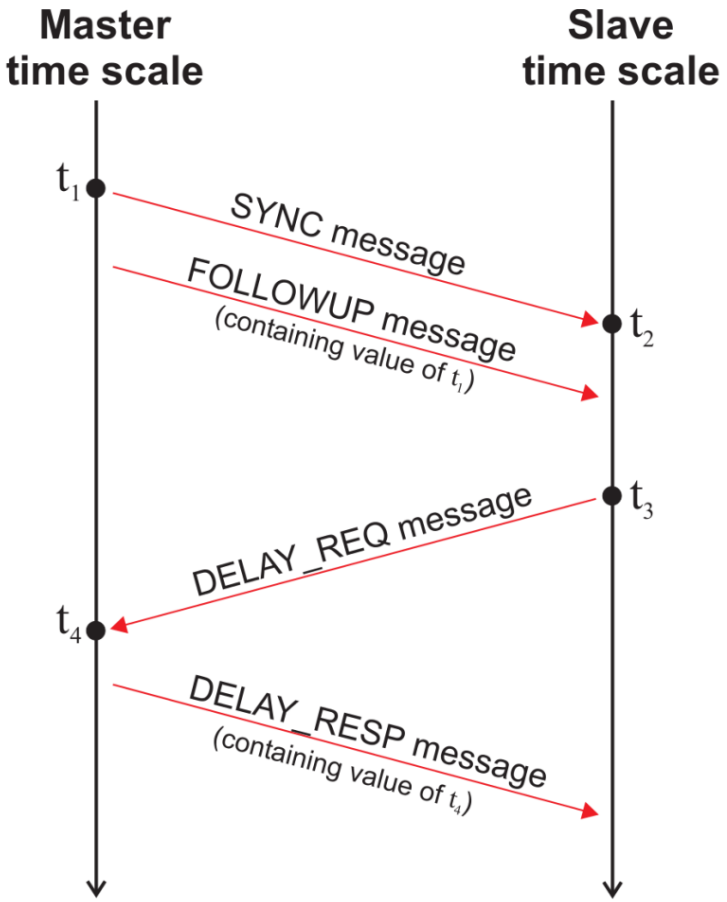
SEVEN Solutions



CPU	
Type	ARM Atmel AT91 SAM9G45
Core	400MHz (ARM926E)
Memories	64MB DDR2 (16-bit bus chip) 256MB NAND flash chip
I/O	32bit Async Bridge with FPGA 100Base-T Ethernet
Software	
OS	Linux (Kernel v2.6.39)
Timing	WRP daemon (node discovery, etc.) PTPv2 daemon
Switching	IEEE802.1x protocols (multicasting, spanning tree, GMRP/-GARP) VLAN Tagging SNMP switch management
Protocols	TCP/IP, SSH, SNMP, NTP, TFTP, DHCP, ARP, DNS

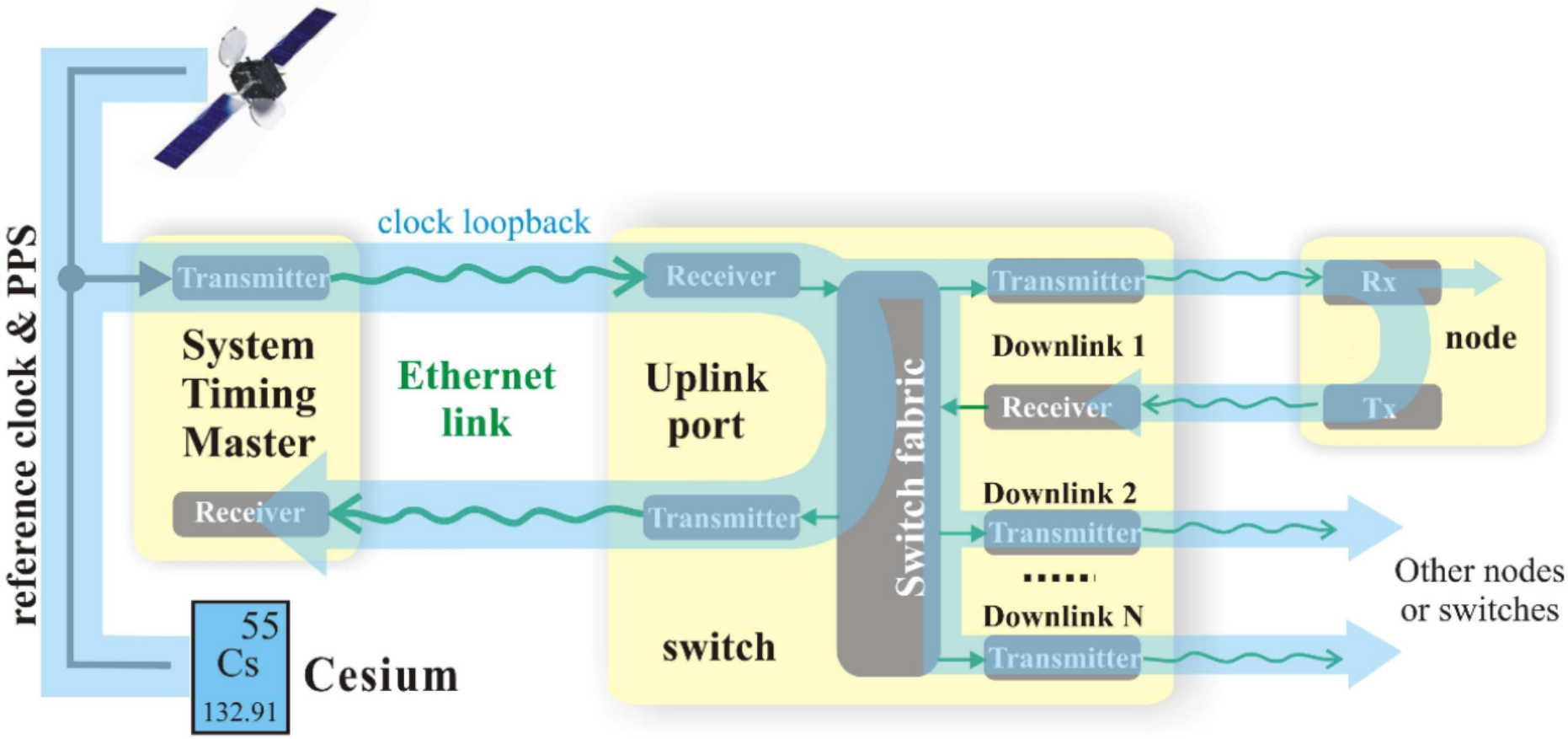
FPGA	
Type	Xilinx Virtex-6 (LX240T)
Package	1156-pin BGA
Slices	37,680 (4 LUTs and 8 flip-flops)
Memories	416x36 Kb Block RAM
Softcore	LatticeMico32 (LM32)
I/0	20 GTX transceivers for SFP links 40 GPIO for generic purpose (LEDs, SFP detection, …)
Monitoring	Monitoring power supply Temperature sensor control
On-Chip Clock Generation	
PLL	AD9516 (14-Output Clock Generator with Integrated 1.6 GHz VCO)
Synthesizer	TI CDCM61002RHBT (28-683MHz)
DAC	2xAD5662BRJ (16bit; 2.7-5.54V)

PTP

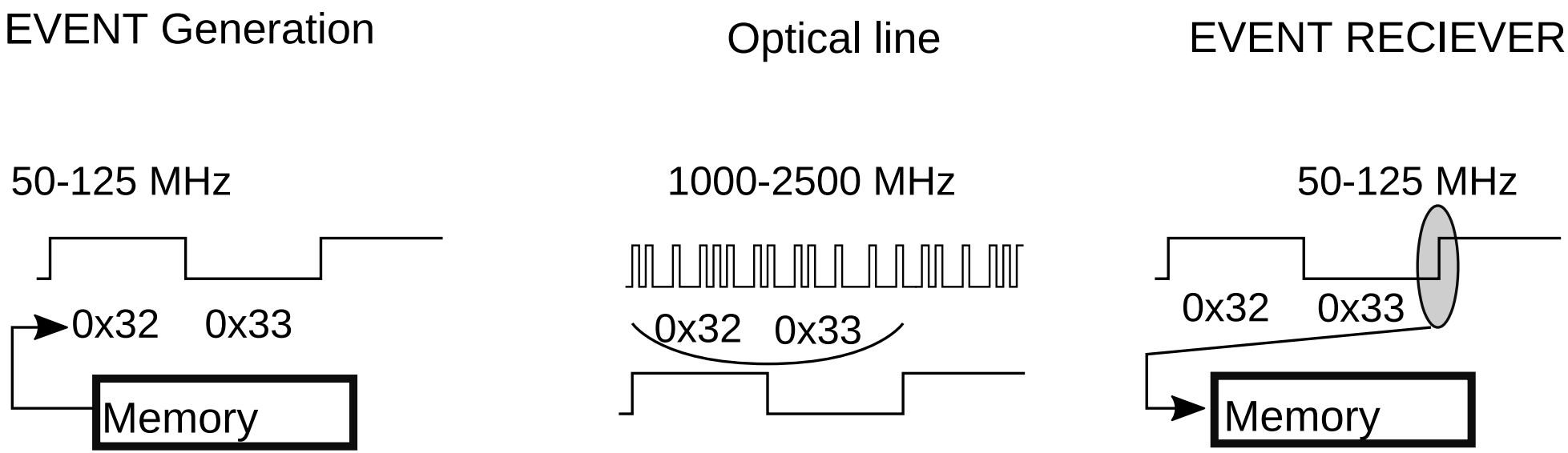


- Frame-based synchronization protocol
- Like NTP but in hardware
- Simple calculations:
  - link *delay*$_{ms}$ $\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$
  - clock *offset*$_{ms}$ $= t_2 - t_1 + \delta_{ms}$

All network devices use the same physical layer cloc
Clock is encoded in the Ethernet carrier and recovered by the receiver chip.
Clock is looped back, phase detection allows sub-ns delay measurement.



Micro-Research Finland Oy

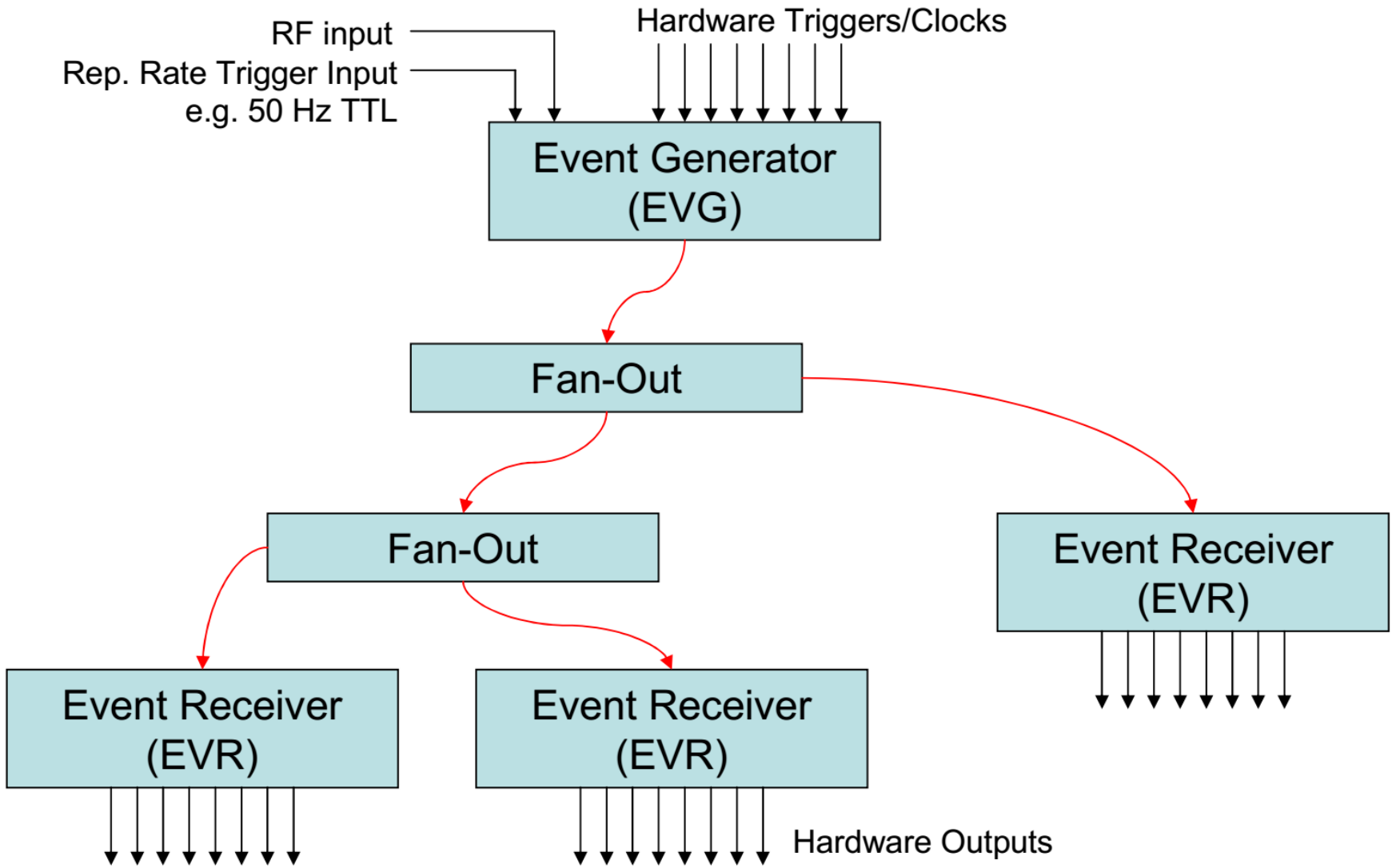


Low-level RF or fractional frequency distribution (50 — 125 МГц)

Event distribution following scenario

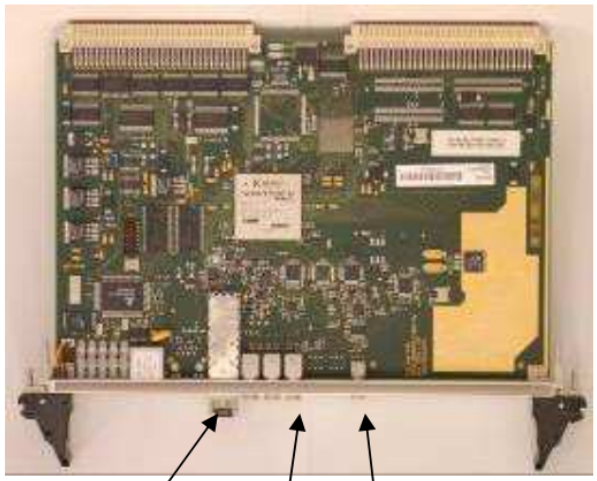
Event Timestamping

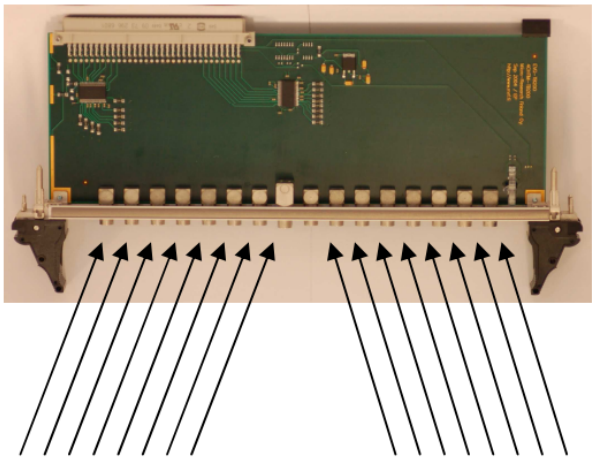
MRF EVG и EVR


RF input
Rep. Rate Trigger Input
e.g. 50 Hz TTL
Hardware Triggers/Clocks
Event Generator
(EVG)
Fan-Out
Fan-Out
Event Receiver
(EVR)
Event Receiver
(EVR)
Event Receiver
(EVR)
Hardware Outputs

VME-EVG-230 VME Event Generator 5352 €

Event Generator (EVG-200)





Distributed bus inputs

External trigger inputs

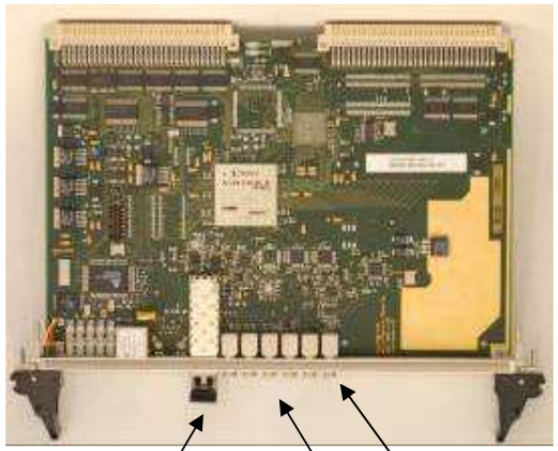
SFP transceiver
• Optical signal to EVRs (fan-outs)

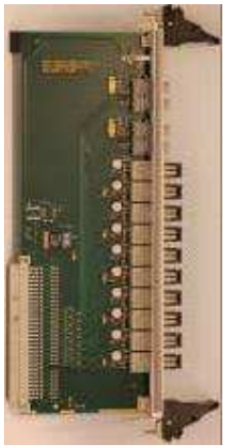
RF input
• Event clock divided from RF
• EVG-200: /4, /5, /6, /8, /10 or /12
• VME-EVG-230: /1, /2, ... , /32

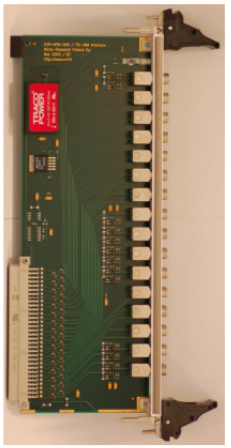
Line syncronisation input
e.g. 50 Hz / 60 Hz TTL level

VME-EVR-230 VME Event Receiver 2606 €

Event Receiver (EVR-200-RF)







HTB OTB TTB NTB

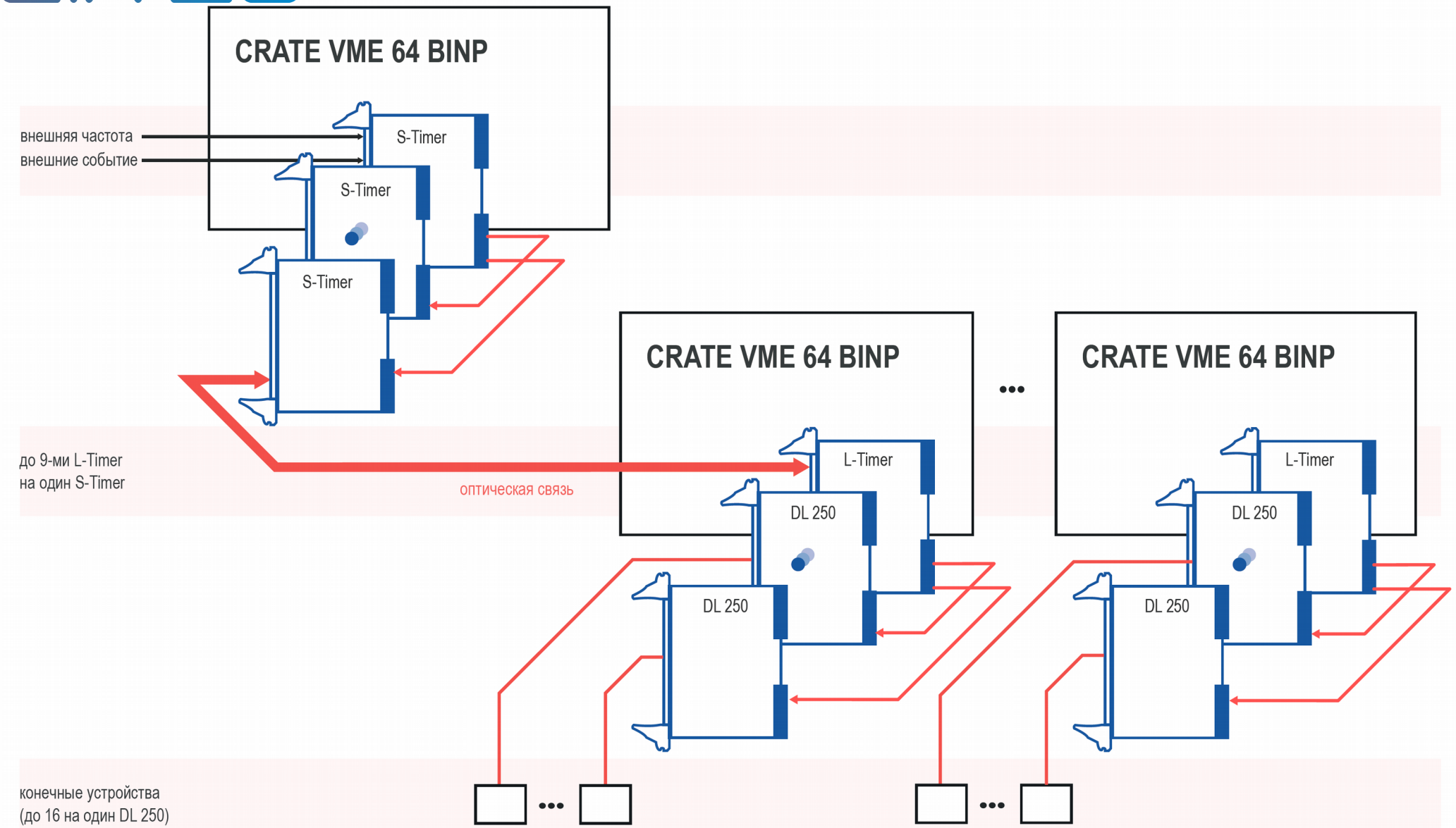
Recovered RF output (optional)

Programmable outputs
- 5 TTL level
- 2 LVPECL level

External trigger input

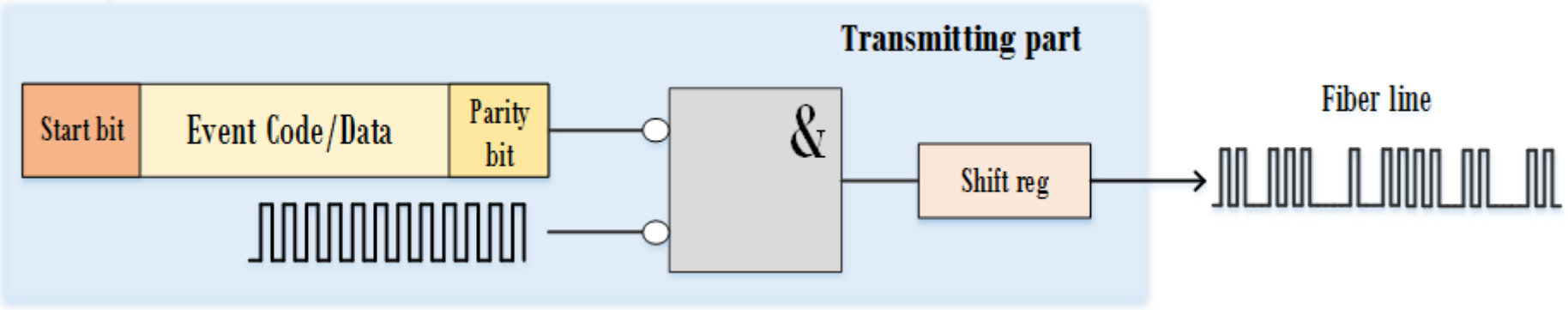
SFP transceiver
- Optical signal from EVG (or fan-out)

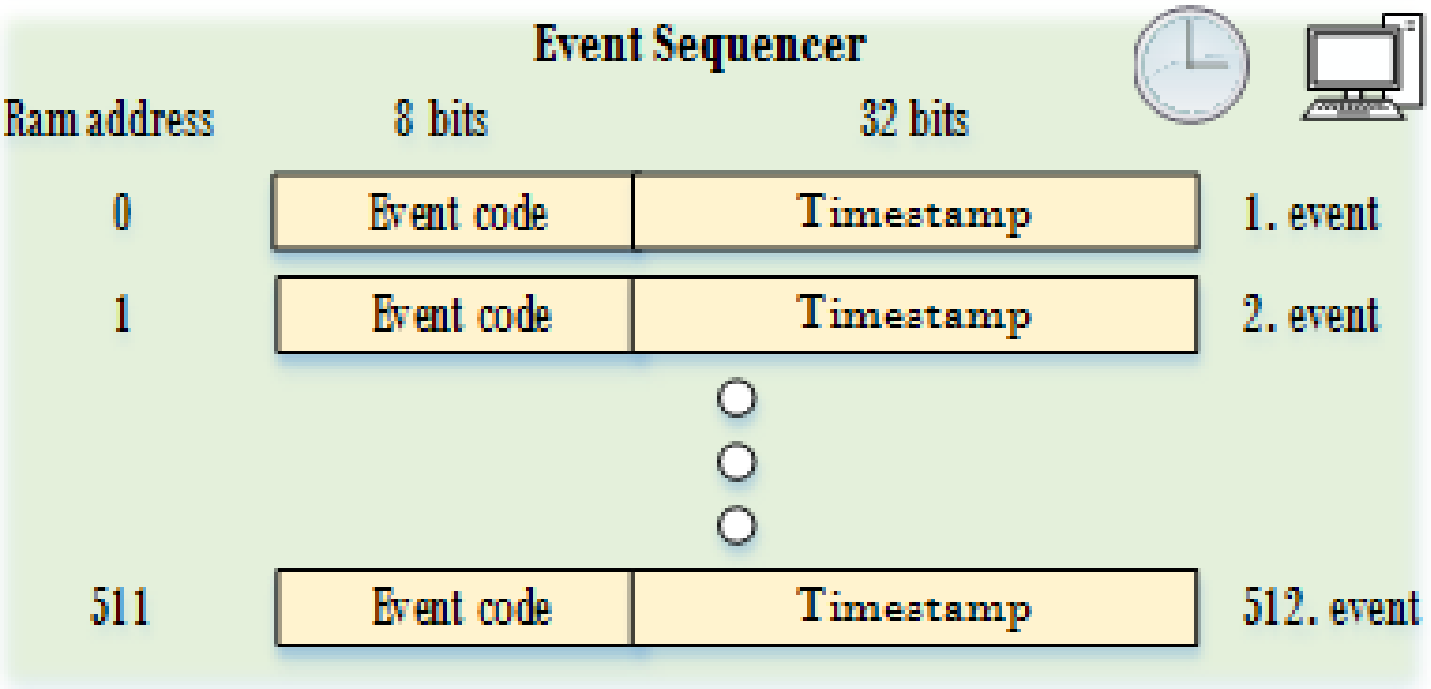
BINP Scheme



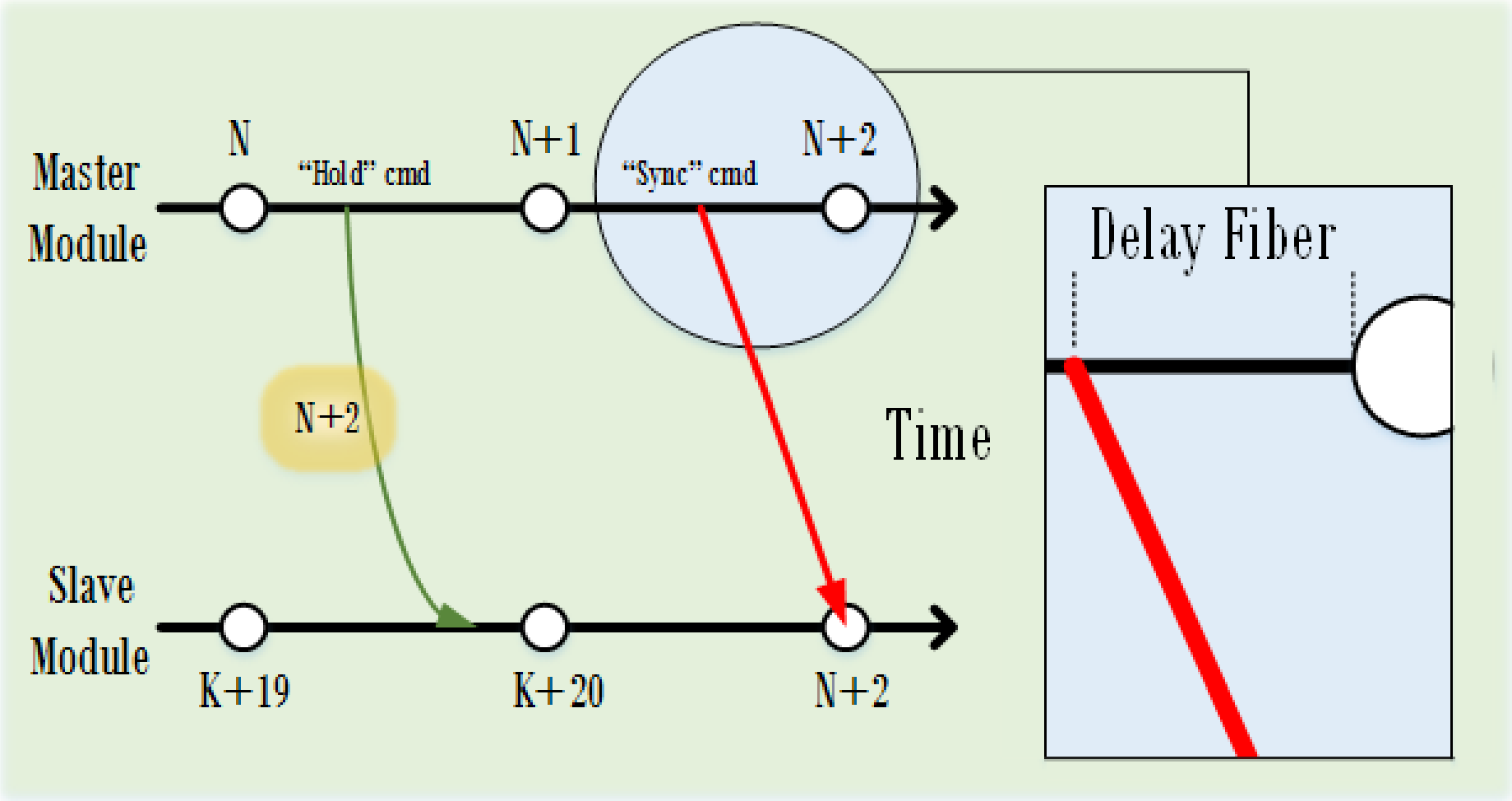
структура системы синхронизации с использованием модулей S-Timer и L-timer

Transmission





Setting the clock

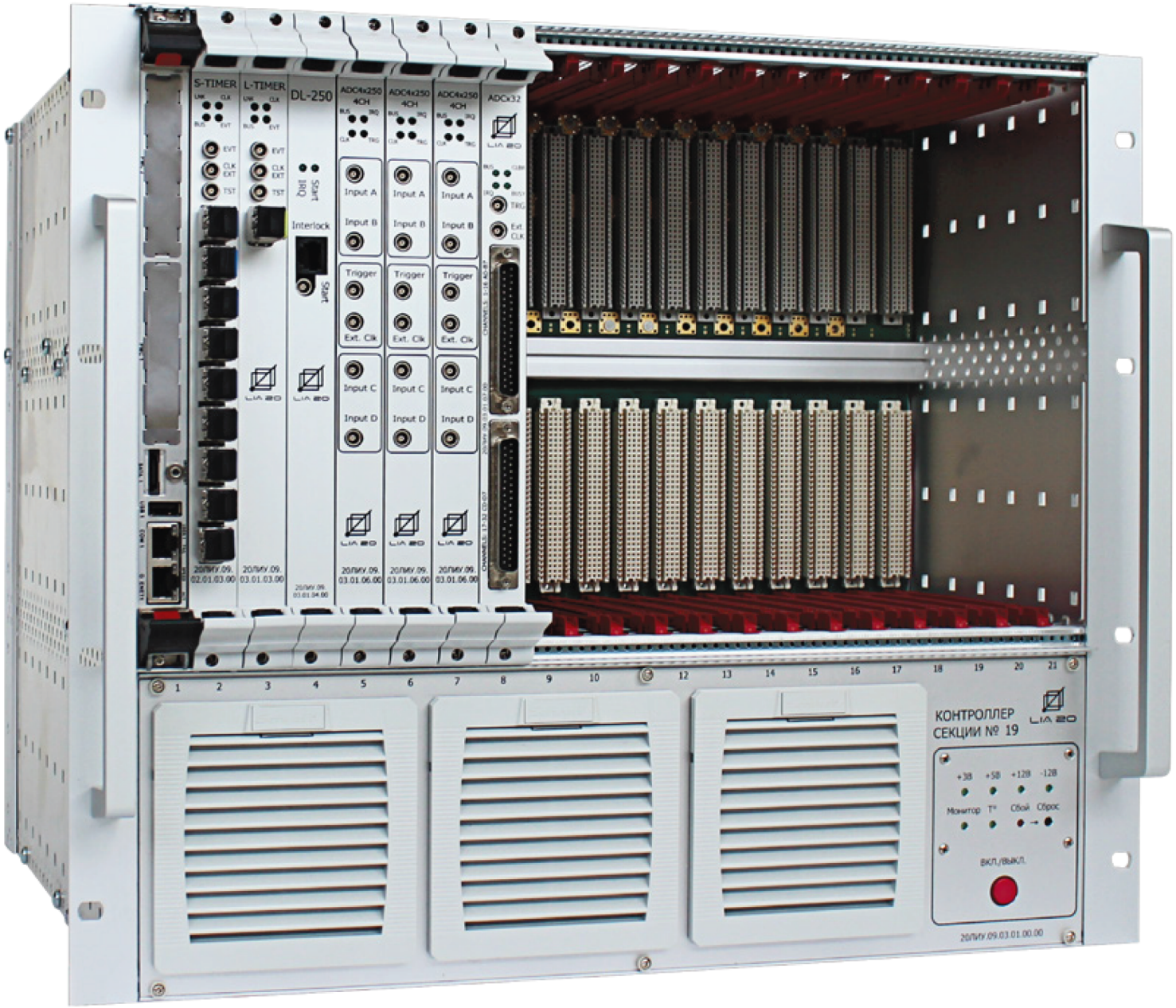


S-Timer

9 output optical lines
2 synchronization inputs
250 MHz clock in
optical lines
±125 ps Delay
measurement error
Jitter < 100 ps
Up to 256 Events
Event Sequencer
Timestamp

L-Timer

1 input optical line
2 synchronization inputs
±125 ps Delay measurement error
Jitter < 50 ps
8 TTL lines with 512 ns length
19 intermodule communication lines


S-TIMER
L-TIMER
DL-250
ADC4x250 4CH
ADC4x250 4CH
ADC4x250 4CH
ADCx32
Input A
Input B
Trigger
Ext. Clk
Input C
Input D
Start
Interlock
КОНТРОЛЛЕР СЕКЦИИ № 19
+3В
+5В
+12В
-12В
Монитор
Т°
Сбой
Сброс
ВКЛ./ВЫКЛ.
2ОЛМУ.09.03.01.00.00