Development of Modern Digital Synchronization Modules at BINP

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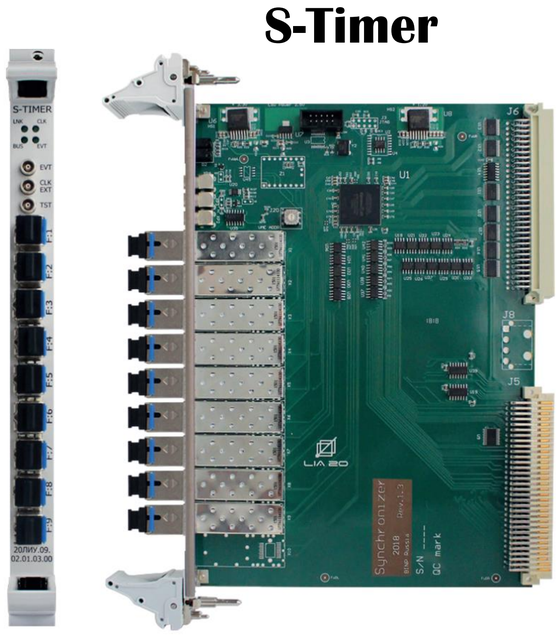
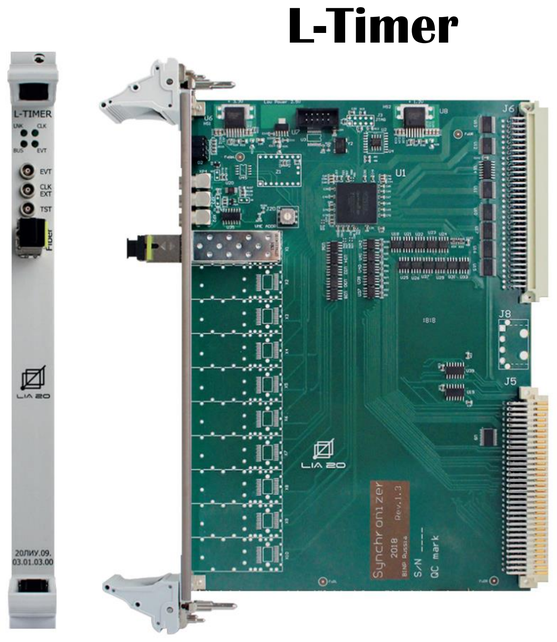
Modern digital synchronization system for big physical facilities is developed at BINP. It allows synchronizing the spatially distributed control devices with an accuracy of ±125 ps and low jitter (< 100 ps). Accurate time distribution and delay compensation is provided, as well as an ability to react to external events with a determined latency. Two modules are used in this subsystem: S-Timer and L-Timer. S-Timer provides a synchronized 250 MHz clock signal with embedded events data through the optical link to nine L-Timers or S-Timers. L-Timer decodes the signal from the optical link and provides synchronization pulses to final control devices.

S-Timer

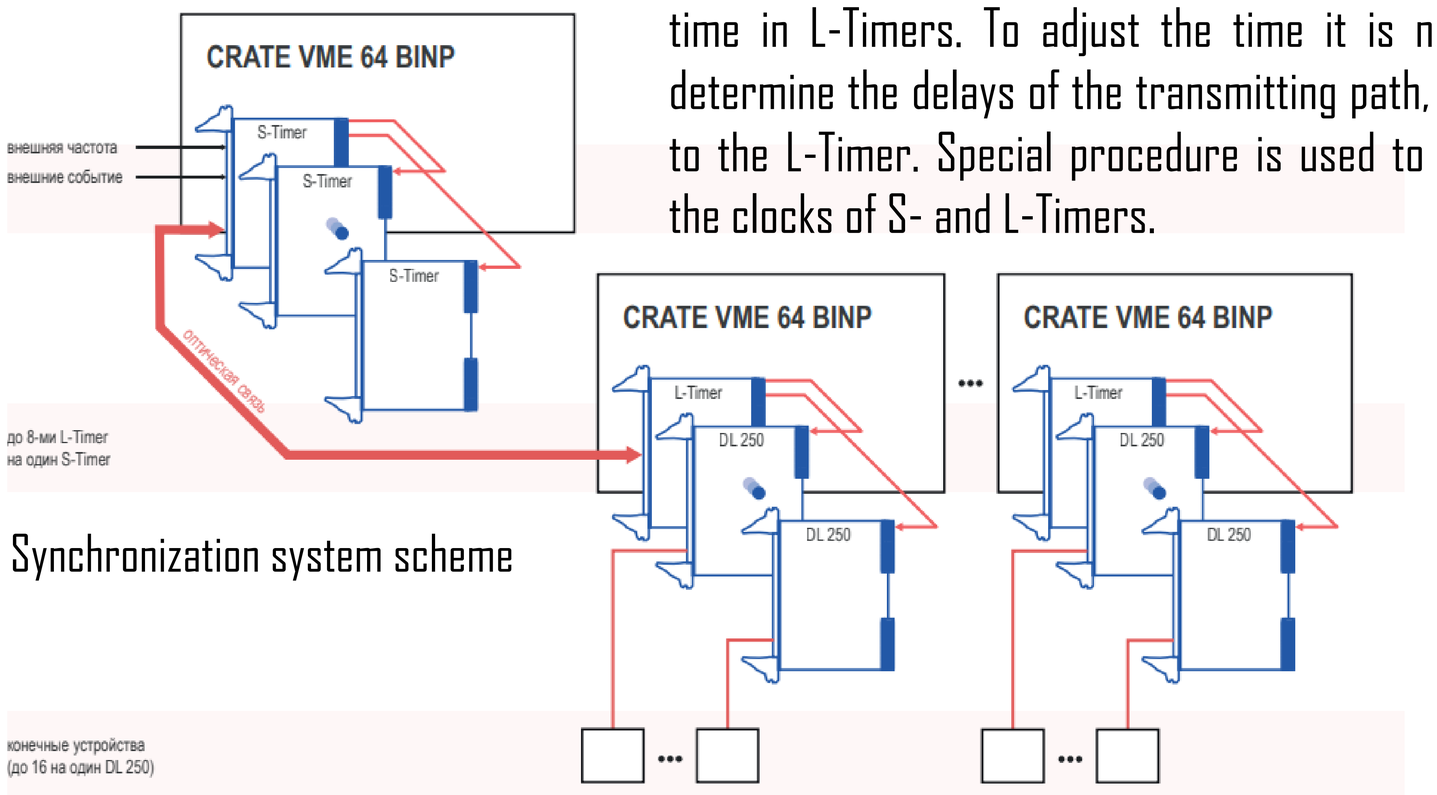


- 9 output optical lines
- 2 synchronization inputs
- 250 MHz clock in optical lines, 250 MHz internal clock
- ±125 ps Delay measurement error
- Jitter < 100 ps
- Up to 256 Events
- 512 Words Event Sequencer
- 512 Words Timespamp

L-Timer

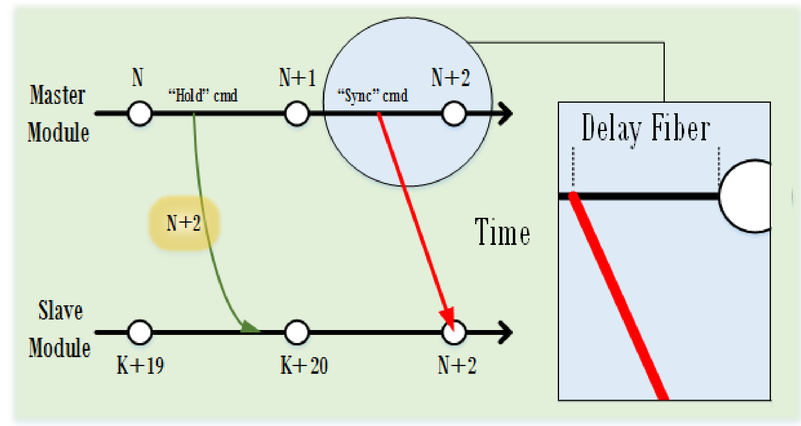


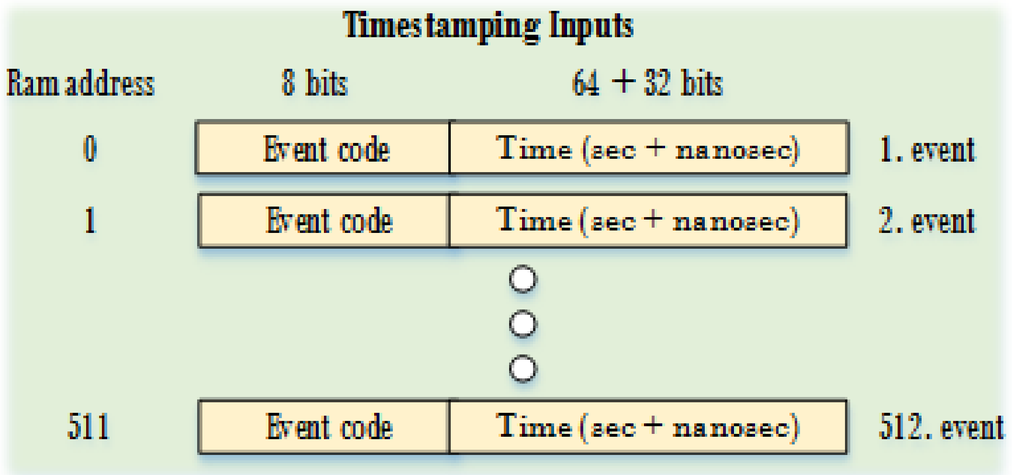
- 1 input optical line
- 2 synchronization inputs
- 250 MHz internal clock
- ±125 ps synchronization error
- Jitter < 100 ps
- 8 TTL lines with 512 ns length
- Synchronization lines CLK125(125 MHz), USRCLK, SYNC
- 19 intermodule communication lines

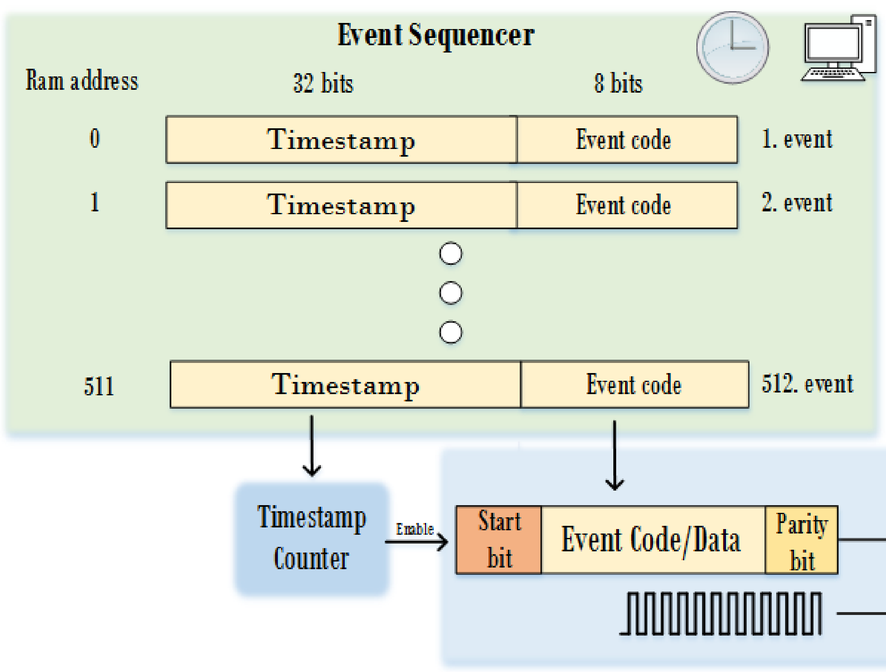


Synchronization system scheme

One of the main tasks of S-Timer is to provide a common time in L-Timers. To adjust the time it is necessary to determine the delays of the transmitting path, then send it to the L-Timer. Special procedure is used to synchronize the clocks of S- and L-Timers.

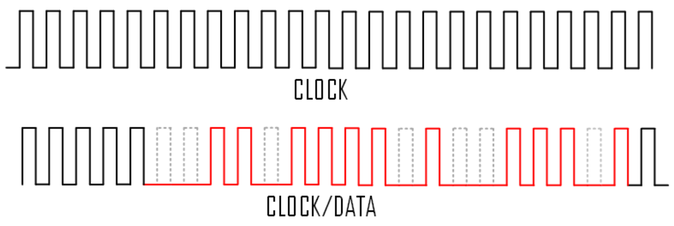


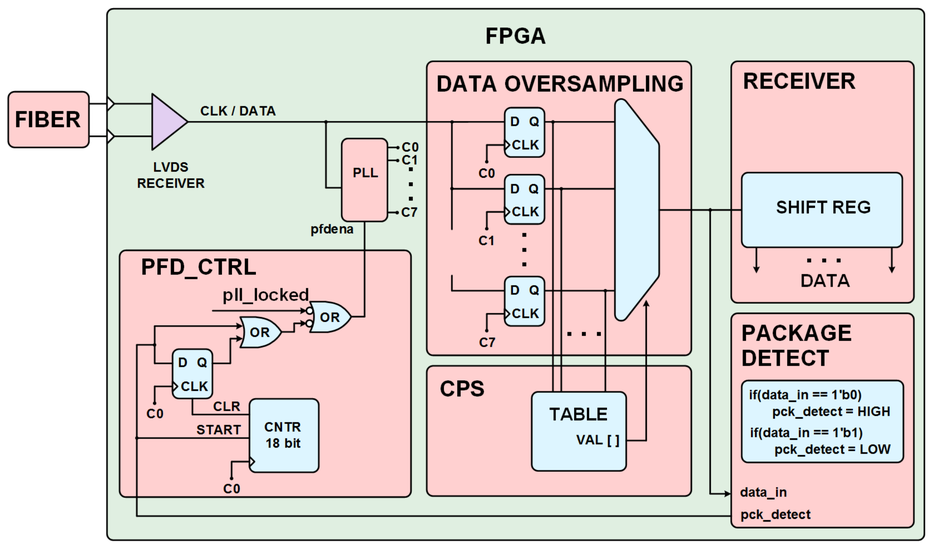




The launch of the "Event Sequencer" is provided in several ways: manual start, or launch on a timestamp at global clock.

Each event sent by the S-Timer module in the optical line is fixed with a timestamp. Each event received by the L-Timer module from the optical line is fixed with a timestamp.





The idea of the packet detection scheme for both modules is to select the phase in advance of the timing signal. The received signal is applied to an array of DFF (DATA OVERSAMPLING), each of which is clocked by a 250 MHz clock signal with a 45 ° offset the adjacent DFF. Trigger outputs are fed to the multiplexer and the location of the CPS phase selection (Clock Phase Selector), which controls the multiplexer. The signal with the multiplexer output is transmitted to the receiver (RECIEVER) and the packet detector (PACKAGE DETECT) and then to the phase detector control circuit (PFD_CTRL).