DEVELOPMENT OF MODERN DIGITAL SYNCHRONIZATION MODULES AT BINP

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Abstract

Modern digital synchronization system for big physical facilities is developed at BINP. It allows synchronizing the spatially distributed control devices with an accuracy of ±125 ps and low jitter (< 100 ps). Accurate time distribution and delay compensation is provided, as well as an ability to react to external events with a determined latency. Two modules are used in this subsystem: S-Timer and L-Timer. S-Timer provides a synchronized 250 MHz clock signal with embedded events data through the optical link to nine L-Timers or S-Timers. L-Timer decodes the signal from the optical link and provides synchronization pulses to final control devices.

INTRODUCTION

One of the important elements for the control of big physical facilities is the synchronization system. The tasks of synchronization systems are transmission of the operating frequency and the transmission of trigger events. The digital synchronization system is developed at BINP that is based on modern principles. It consists of two types of modules: S-Timer and L-Timer. These modules allow synchronizing the spatially distributed control devices with an accuracy of ±125 ps and low jitter (< 100 ps) as shown in Fig. 1. Special VME-BINP [1] synchronization lines are used for communication between modules in the same crate.

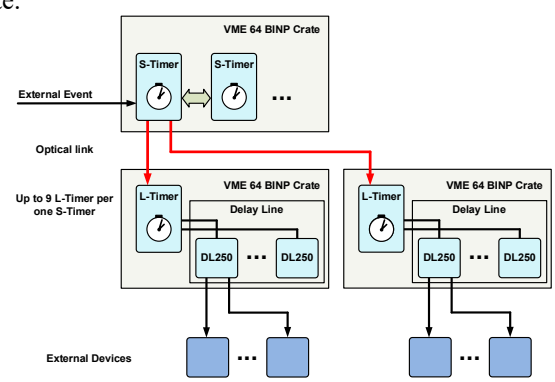

Figure 1: Synchronization structure using S-Timer and L-Timer modules.

S-Timer (Fig. 2) provides a synchronized 250 MHz clock signal with embedded events data through the optical lines to up to 9 L-Timers. The S-Timer has an input to receive a precise external clock or external events. Several S-Timers can be united in one crate. The L-Timer decodes the signal from the optical line and provides all necessary synchronization pulses to the modules of the crate. Both modules use the same PCB with different montage.

S-TIMER

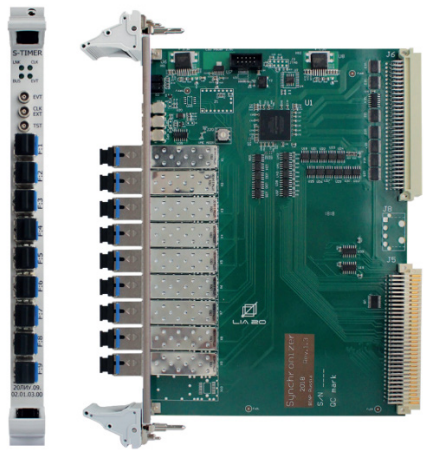

Figure 2: S-Timer module.

The main characteristics of S-Timer are:

- 9 output optical lines
- 2 synchronization inputs
- 250 MHz clock in optical lines
- ±125 ps Delay measurement error
- Jitter < 100 ps
- Up to 256 Events
- 512 Words Event Sequencer
- 512 Words Timestamp

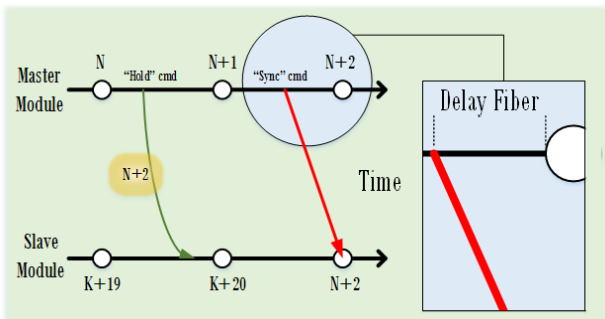

Figure 3: Common time diagram.

One of the main tasks of S-Timer (Master module) is to provide a common time in L-Timers (Slave module). To adjust the time it is necessary to determine the delays of the transmitting path, and then provide this information to the L-Timer. The special procedure is used to synchronize the clocks of S- and L-Timers that shown in Fig. 3. Master module fixes the L-Timer's current time by the command "Hold". Next step is to add 2 seconds to the fixed Master

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time. The obtained value is transferred to the Slave module and is saved in its clock register. Then the “Sync” command is given taking into account the line delay so that the Slave timer starts counting from the same value N+2 as the Master’s one.

The events transmitting diagram shown in Fig. 4. The transmission protocol consists of one start bit, 16 data/event code bits (8+8) and one parity bit. The protocol can be used to transmit up to 256 codes with data values.

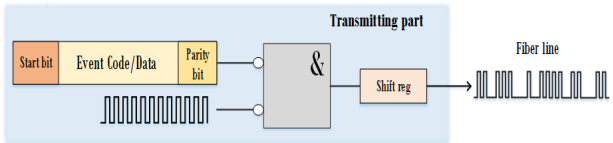

Figure 4: Events transmitting diagram.

The S-Timer provides the possibility of sequential triggering of events as shown on Fig. 5. The events are generated according to the table called "Event Sequencer" tha contains the event code and the delay. The size of the table allows programming the sequence of up to 512 events. The launch of the sequence can be initiated manually, or at a certain time.

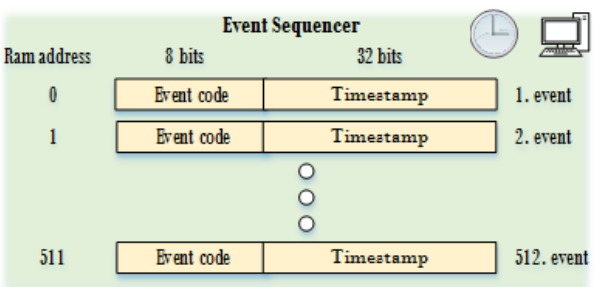

Figure 5: Event Sequencer diagram.

L-TIMER

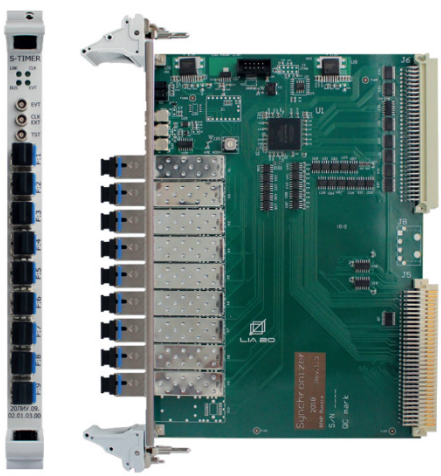

Figure 6: L-Timer module.

The main characteristics of L-Timer (Fig. 6) are:

- 1 input optical line
- 2 synchronization inputs
- ±125 ps Delay measurement error
- Jitter < 100 ps
- 8 TTL lines with 512 ns length
- Synchronization lines CLK125(125 MHz), USRCLK, SYNC
- 19 intermodule communication lines

The synchronization lines include CLK125, USRCLK and SYNC. They are used to transfer a common 125 MHz clock, common user-defined clock and a precise synchronization pulse respectively.

The module provides a buffer of 512 timestamps for events shown on Fig. 7. Each event received by the L-Timer module from the optical line is fixed with a timestamp in seconds and nanoseconds.

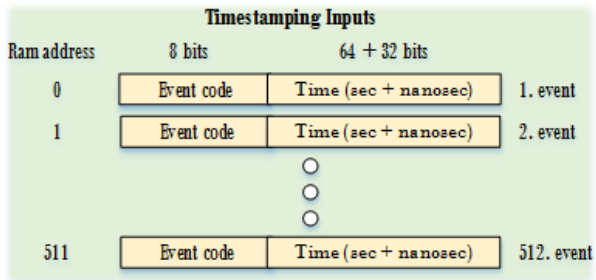

Figure 7: Timestamping input diagram.

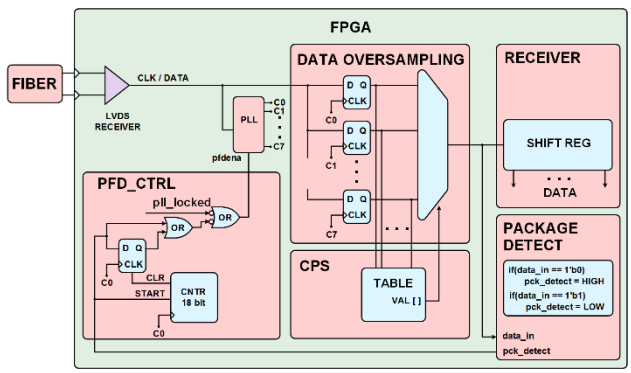

Figure 8: L-Timer detection scheme.

The idea of the packet detection scheme for both modules is to select the phase in advance of the timing signal shown in Fig. 8. The received signal is applied to an array of DFF (DATA OVERSAMPLING), each of which is clocked by a 250 MHz clock signal with a 45 °offset the adjacent DFF. Trigger outputs are fed to the multiplexer and the location of the CPS phase selection (Clock Phase Selector), which controls the multiplexer. The signal with the multiplexer output is transmitted to the receiver (RECIEVER) and the packet detector (PACKAGE DETECT) and then to the phase detector control circuit (PFD_CTRL).

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SUB-NANOSECOND SYNCHRONIZATION

To provide the sub-nanosecond synchronization a highly accurate FPGA-based phase measurements technique is implemented in the S-Timer and the dynamic phase shifting feature is implemented in L-Timer (Fig.9).

The sync signal 250MHz, which is transmitted by S-Timer for the master-slave synchronization, is redirected back from L-Timer. Then the S-Timer measures the phase difference between transmitted synch signal and received one. This difference is sent by event transmission protocol over the optic line from master to slave module, where the latter one provides phase compensation.

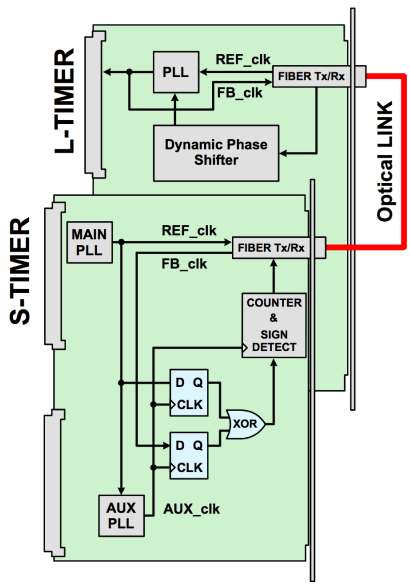

Figure 9: Block diagram of sub-nanosecond phase compensation.

The basic idea of a highly accurate phase measurement technique that is called DDMTD resembles stroboscopic measurements [2] [3]. The reference (S-Timer) and feedback (L-Timer) clock signals are gated by two DFFs on the auxiliary clock frequency, which is slightly different from the reference one. This clock signal is generated from reference clock 250MHz using auxiliary PLL with a factor 128/129. Thus the phase shift is transformed from the high frequency domain into the low frequency one, as a result the time difference is expanded up to values that can be accurately measured using a counter. The time diagram of this method is shown on Fig. 10. The counter is incremented while XOR signal is in high state and is cleared by the positive edge of the reference clock (REF_EXPND). The relationship between the counter value and the phase difference is defined by eq.1. The measurement precision is determined by eq.1. with the minimum value of the counter.

$$t_\varphi = COUNT\_VAL \cdot 15.625\ pS \quad (1)$$

$$\delta_\varphi = t_\varphi[@\ COUNT\_VAL = 2] = 31.25\ pS \quad (2)$$

The phase compensation on L-Timer side is based on the PLL dynamic reconfiguration feature of Altera Cyclone III FPGA [4]. This feature allows changing the phase of PLL output clock in real time with the step that equals 1/8 of the voltage controlled oscillator (VCO) frequency. This is realized by incrementing or decrementing the feedback counter of PLL. The VCO of L-Timer PLL oscillates with 1GHz frequency, thus the accuracy of the adjustment is ±125ps.

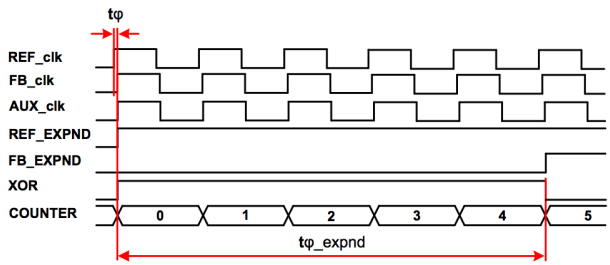

Figure 10: Time diagram of the stroboscopic phase measurement.

CONCLUSION

Two modules were developed at BINP for synchronization subsystem: S-Timer and L-Timer. They allow synchronizing the spatially distributed control devices with an accuracy of ±125 ps and low jitter (< 100 ps). This synchronization structure will be used at Linear Induction Accelerator LIA-20 [5], and can be used in other large-scale installations.

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