VME BASED DIGITIZERS FOR WAVEFORM MONITORING SYSTEM OF LINEAR INDUCTION ACCELERATOR LIA-20

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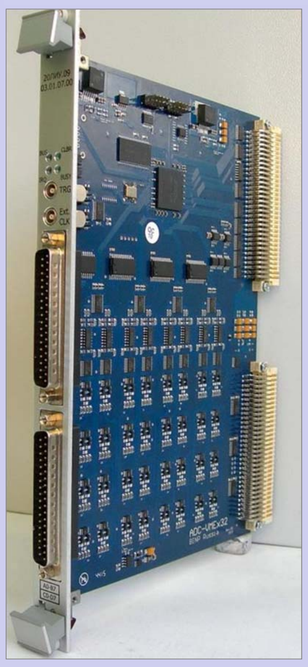
The Linear Induction Accelerator LIA20 is being created at the Budker Institute of Nuclear Physics. Waveform monitoring system (WMS) is an important part of LIA20 control system. WMS includes "slow" and "fast" monitoring subsystems. "Slow" subsystem provides monitoring of processes with typical duration about 500 μs – 20 ms. "Fast" subsystem is able to record processes with duration about 10 ns – 400 ns. Three kinds of digitizers have been developed for WMS. "Slow" subsystem based on ADCx32 and “fast” one based on two types of digitizers ADC4x250-4CH and ADC4x250-1CH.

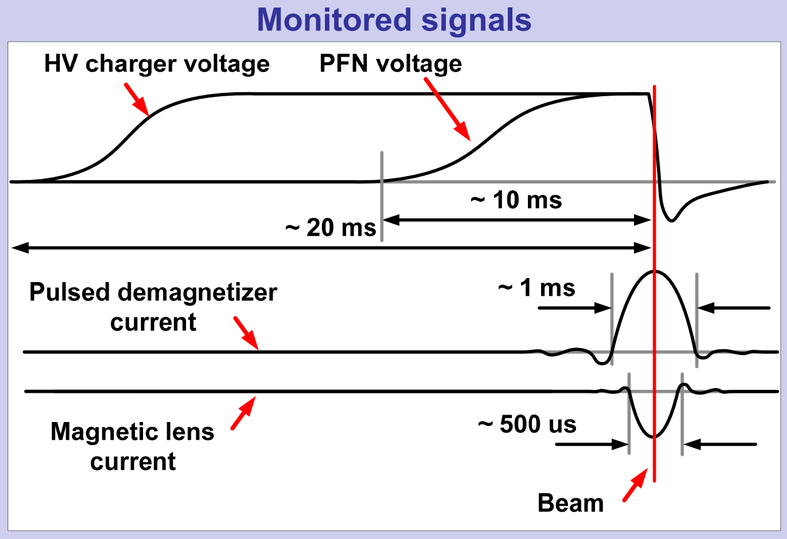
SLOW DIGITIZERS ADCx32



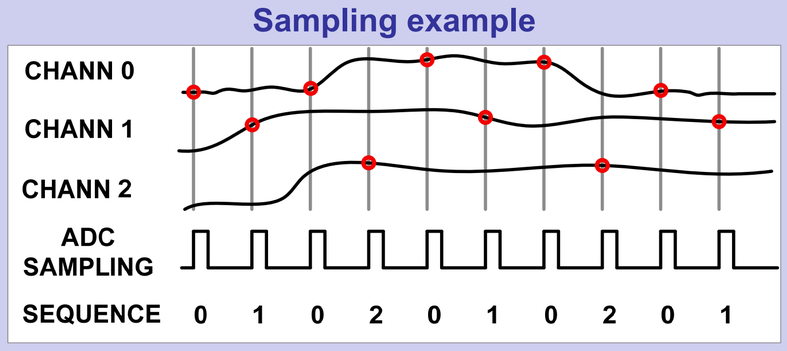
ADCx32 provides measurements of such parameters as HV charger voltage, PFN voltage, demagnetizer current and magnetic lens current of LIA-20 Pulsed HV System with 1540 total number of channels and 500us – 20ms time range.

The basic idea of ADCx32 design is using four 8 channel multiplexed 1 MSPS SAR ADCs with programmable channel sequencing. Channel sequence configuration determines sampling rate for each ADC channel individually. That allows sampling channels with shorter time duration faster than channels with longer time duration. This approach is illustrated in the right figure. Sequence example is shown in timing diagram for the case, when CH.0 of ADC records fast process with twice higher sampling rate than CH.1 and CH.2.

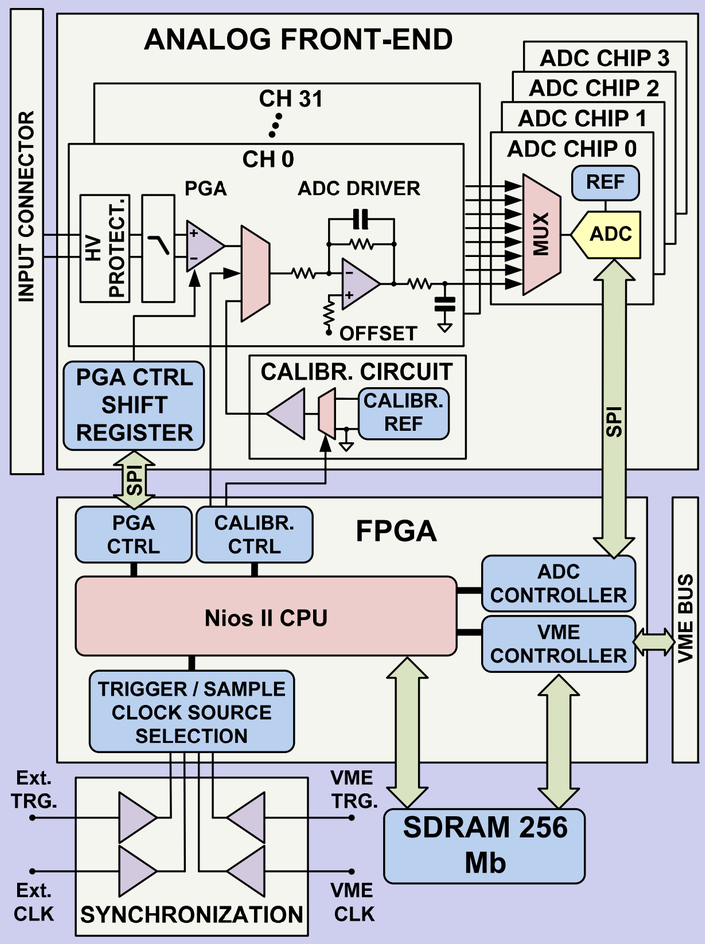
Monitored signals



Sampling example

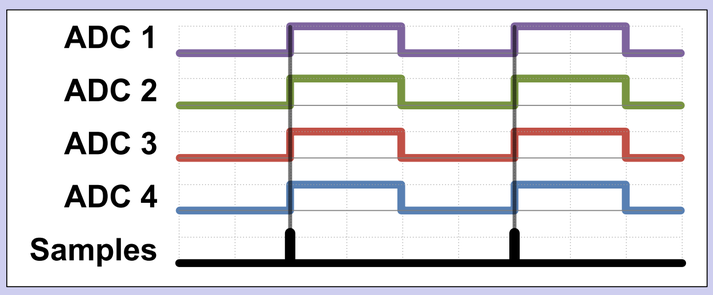


ADCx32 structure

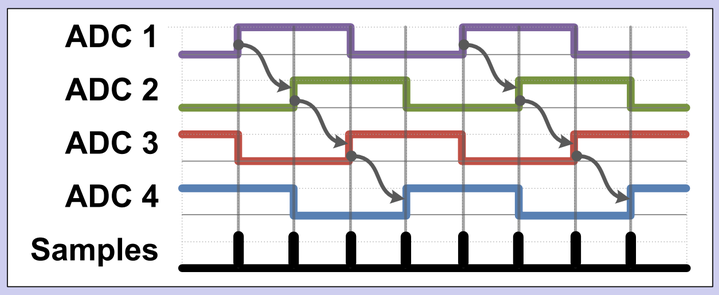


FAST DIGITIZERS FAMILY ADC4x250

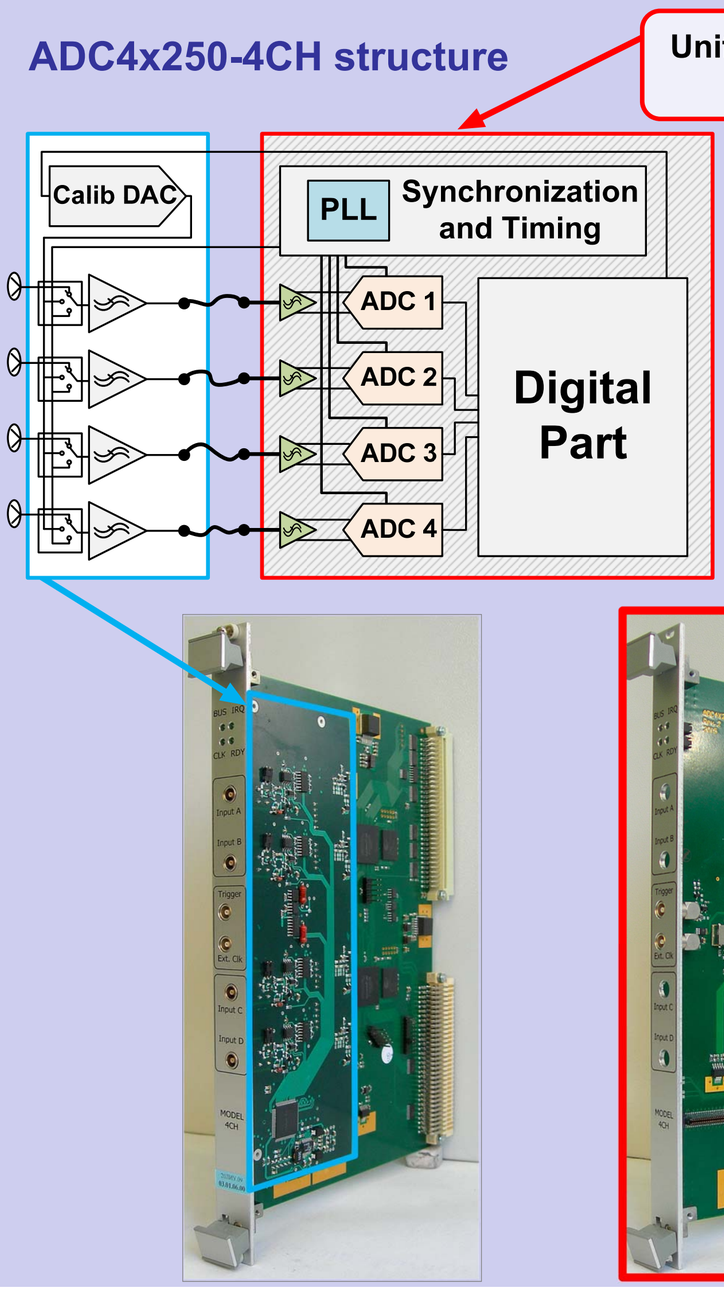
ADC4x250-4CH relation of ADC clocks



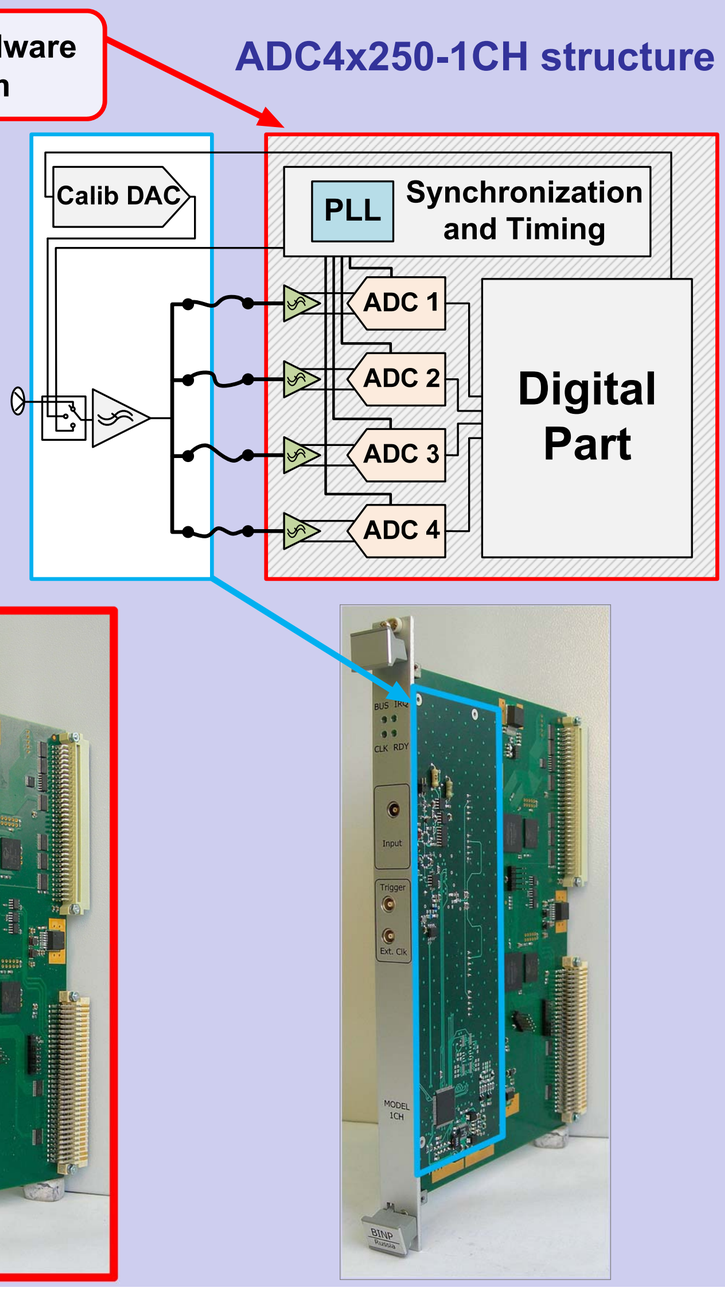
ADC4x250-1CH relation of ADC clocks



ADC4x250-4CH structure



ADC4x250-1CH structure



ADC4x250 is set of two devices. The first of them is four-channel 250 MSPS digitizer ADC4x250-4CH. Its structure is shown on the left side of illustrate. And the second one is one-channel device with performance of 1000 MSPS shown on the right and named ADC4x250-1CH.

Red color marked part of structures is unified hardware platform. Its implemented in 8-layers PCB in VME 6U standard and its identic for both digitizers. The difference in devices is input amplifiers board that stacked with platform board as mezzanine extension. They are marked by blue color in image and are implemented in 4-layers PCB in a much more simple way than platform board.

Also firmware reconfigures clock circuit when another amplifier part is connected for realize time interleaved scheme of A/D conversation.

It means that for four-channel device all ADCs are driven by synchronous clocks and corresponds to its own input channel. Sample rate of such device coincides with the sample rate of one ADC and equals 250 MSPS.

For one-channel device ADCs is driven by clock signals with a phase shift of 90° and work sequentially in time. It allows to multiply sample rate of one ADC by four and gain summary sample rate equal 1000 MSPS.

Of course, there is additional error inherent to this method. Because of this, advanced calibration and signal processing stage are realized in firmware of one-channel module.

	ADC4x250-4CH	ADC4x250-1CH
Sampling rate	250 MSPS	1000 MSPS
Bandwidth, -3dB	75 MHz	300 MHz
Numb. of channels	4 simultaneously	1
Voltage ranges	±0.5 V, ±1 V, ±2 V, ±4 V	
Resolution	12 bit	
Buffer length	786 432 samples/ch	3 145 728 samples/ch
Static noise (RMS)	< 0.8 LSB	< 1 LSB
Phase noise (RMS)	< 0.7 ps	< 0.7 ps
Crosstalk	< -60 dB at 50 MHz	—
SNR	62.7 dB_{FS} at 11 MHz	62 dB_{FS} at 110 MHz
SINAD	61.8 dB_{FS} at 11 MHz	45.6 dB_{FS} at 110 MHz