A DIGITAL LOW-LEVEL RF SYSTEM FOR RESONANT BEAM DEFLECTOR OF LAPLAS EXPERIMENT

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Abstract

A two-resonator heavy ion deflecting system is a part of LAPLAS experiment [1]. ITEP built and put into operation a lightweight prototype of a deflector. Developed high performance radio-frequency control unit provides all necessary options for successful operation in LAPLAS or ITEP installations. The LLRF includes a two-channel reference generator based on a digital signal processing core and resonant frequency control modules, also powered by an appropriate DSP.

RF DEFLECTOR

ITEP develops a radio-frequency deflector of high-energy heavy ion beams as a prototype of the system, assigned to plasma physics experiment in FAIR (Darmstadt, Germany). The operating prototype, shown in Fig.1, consist of two resonators forming orthogonal electromagnetic fields to deflect the beam in vertical and horizontal planes and provide a cylindrical impact volume in solid target body.

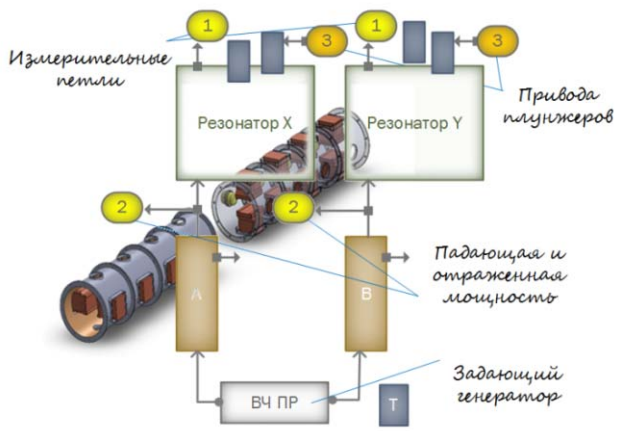

Figure 1: RF system of the beam deflector.

LOW-LEVEL RF SYSTEM

Fig. 2 shows the LLRF divided into the measurement and generator parts. The LLRF system of the deflector operates in conventional way, similar to LLRF systems of resonant accelerators. As a reference generator, it issues two coherent RF signals, shown as outputs A and B in Fig. 3. When required, the amplitude of signals could be independently set within full-scale range. The ability of the phase difference control between channels is a key option of the reference generator. The phase is adjustable in the 360-degree range. The feedback controller allows phase correction on pulse-by-pulse base.

The model of the RF system of the deflector use three independent parameters describing the system: resonant frequencies and a phase difference between two resonators. The system uses a set of control signals to stabilize the model near the optimal statement. The main criteria of the proper system operation are accurate phases and amplitudes of EM fields, estimated by measuring of signals taken from control loops 1_X and 1_Y in Fig. 1. Signals 2_X and 2_Y from reflectometers are used while checking the matching criterion.

Fig. 2 presents the structure of the crate of the LLRF module.

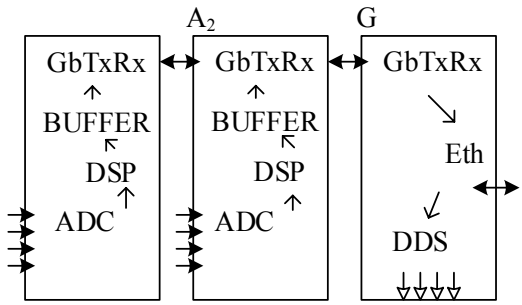

Figure 2: The structure of the LLRF module.

The crate unites two similar four-channel ADC modules A1 and A2, capable simultaneously digitize RF signals in the IF mode, and vector signal synthesizer G with pair of independent two-channel outputs of sinusoidal signals.

GENERATION OF REFERENCE SIGNALS

As shown in Fig. 3, the output signals are generated using the frequency up converter scheme.

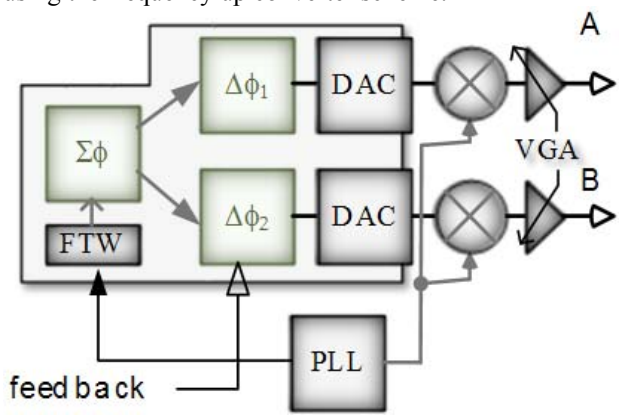

Figure 3: The reference generator.

Two-channel DDS generates synchronized signals of intermediate frequency. The frequency depends on frequency tune word (FTW) and frequency of the synchronization clock taken from on-board PLL-based synthesizer. The PLL's voltage controlled oscillator (VCO) generates the frequency of 1740 MHz. The clock

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signal of ¼ of the VCO feed the DDS. The integrated two-channel DDS on single chip is an optimal solution because it provides flexible signal generation combined with seamless synchronization mechanism and simple control interface. 14-bit phase words $\Delta\phi_1$ and $\Delta\phi_2$ define phases of output signals with less than 0.025° step.

Two outputs of PLL serve as local oscillators (LO) for up converters. This configuration define the output frequency of generator as follows:

$$f_{OUT} = \left(\frac{FTW}{2^{32}} \frac{1}{N_1} + \frac{1}{N_2} \right) f_{VCO} \qquad (1)$$

where N_1 and N_2 are frequency division coefficients for the DDS synchronization and LO outputs of the PLL. As it follows from the formula 1, the required output frequency may be obtained in several ways, and this allows an additional optimization in terms of intermodulation components.

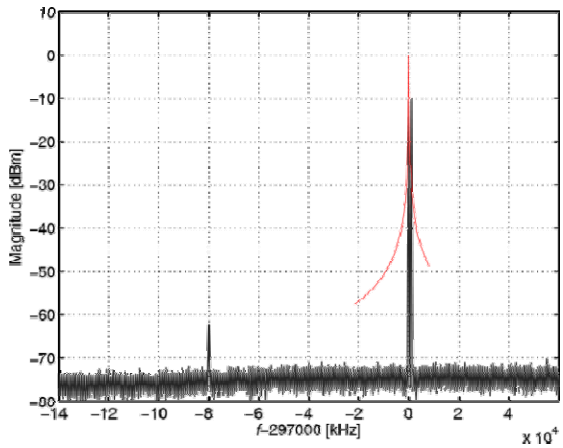

Figure 4: The output spectrum of the reference generator.

Fig. 4 shows the measured spectrum at the generator output. In the figure, the spectrum superposed the frequency characteristic of a resonator. One can see the nearest peak of the spurious signal, which is pretty far out of the system central frequency.

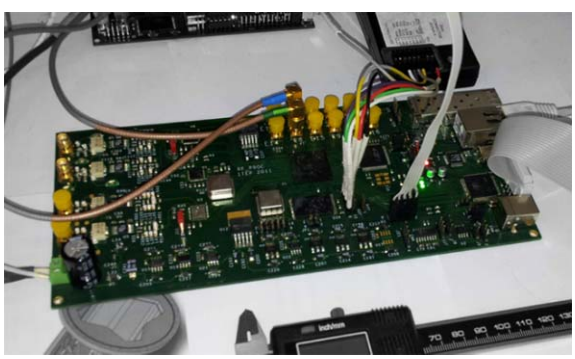

Figure 5: The PCB of the reference generator.

Fig. 5 shows the assembled printed board of the reference generator. Analog components: DDS, mixers, filters, transformers and variable gain amplifiers occupy the left side of the board. The FPGA microchip and supplemental components are placed in the central area to have shortest paths to analog circuits and high-speed serial interface connectors, placed on top of the PCB. The FPGA implements a control logic for board periphery configuration, for the signal processing and for local data exchange between the generator and ADC modules. The long-distance communication use a lightweight ARM microprocessor to provide the remote control and data delivery to the host computer over TCP/IP protocols. The microprocessor and communication related stuff take the right side of the PCB. Fig. 5 shows the board connected to the FPGA and ARM JTAG programmers.

Table 1 gives main parameters of the vector reference generator.

Table 1. main parameters of the vector reference generator.

Operating frequency f_0.	MHz	297
Frequency range. (not less)	MHz	f_0±0.5
Frequency tune step.	kHz	<0.1
Long-term frequency stability.	kHz	±3
Amplitude range.	dBm	-52÷-3
Amplitude range with VGA	dBm	-31÷18
Phase range.	Degree.	0÷360
Phase tune step.	Degree.	<0.2

SIGNAL MEASUREMENTS

Fig. 6 presents the image of the assembled printed board of the ADC module. The aim of the module is a digitizing of a narrowband signals modulated by 297MHz. Used AD converter has a data rate limited by hundred samples per microsecond, and therefore pair of two-channel 16-bit analog to digital converters operates in intermediate frequency mode.

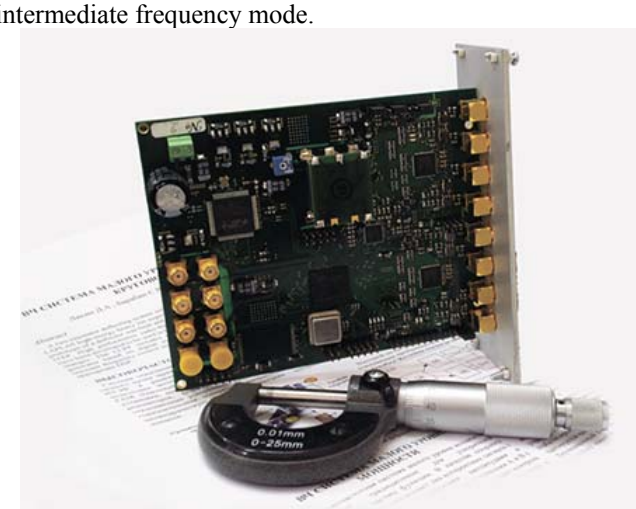

Figure 6: The ADC module.

As it is shown in Fig. 7 the ADC has a sampling rate lower than the input signal carrier frequency and operates as a zero-order hold undersampling device. As a result, the ADC shifts the 12.25 MHz-wide band around the input signal to low frequencies. The shift is equal to

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frequency of 12th harmonic of the sampling clock. The RF system of the deflector, resonators and power RF amplifiers, have a narrow spectrum with no power in the near of the ADC clock harmonics with order other than 12. In addition, an analog pass band filter reduces all possible out of band EMI components of the signal. Consequently, the output of the ADC provides clear and oversampled digital signal with intermediate frequency of 3 MHz. Report [2] describes further data evaluation in details.

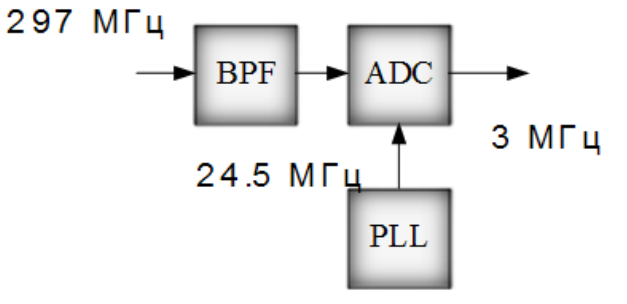

Figure 7: Analog to digital conversion using the IF mode.

SYSTEM INTEGRATION

A high-speed serial interface integrates the reference generator and ADC boards into the single joint module. Fig. 8 shows a logical structure of the whole system. The ADC or detector (D) boards acquire control signals and present the data to the generator (G) block. Detector modules have an interface to the general stepper controller module to adjust the resonant frequency of deflecting resonators using mechanical tuners T.

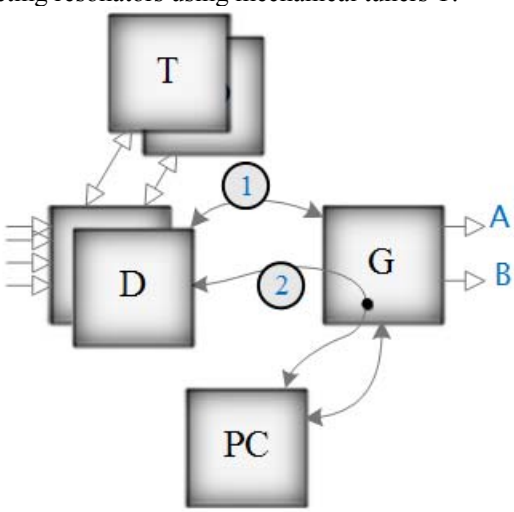

Figure 8: The logical structure of the LLRF.

As it is shown in Fig. 8, LLRF is able to operate as standalone device (branch 1) or could be taken under control by the remote host computer PC (branch 2).

FIRMWARE

The firmware part of the LLRF system includes FPGA and microprocessor microcode for each board, described above. Roughly, the FPGA is logically divided into interface modules, peripheral control modules, timing elements and signal processor. The signal evaluation algorithms is described in [2].

CONCLUSION

Fig. 9 shows the photo of the LLRF module developed for the ITEP version of the RF deflector. At the beginning of 2014 the module was used during the comissioning of the RF deflector.

Figure 9: LLRF module.

Parameters of the developed LLRF allows using it also in RF system of LAPLAS. The operating frequency of klystrons of 354 MHz lies within the range of ADCs and frequency converters. To change the frequency, it would be enough to replace input and output pass-band filters. Then the actual frequency change will be obtained by adjusting of parameters of the formula 1, and tuning of the DSP algorithms.

REFERENCE

[1] S.Minaev et al. 'Multi-cell RF deflecting system for formation of hollow high energy heavy ion beam', proc. IPAC10, Kyoto, Japan.
[2] D.Liakin et al. 'Digital signal processing algorithms for linac low-level RF systems', this proc.

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