DIGITAL SIGNAL PROCESSING ALGORITHMS FOR LINAC LOW-LEVEL RF SYSTEMS

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Abstract

A set of LLRF systems had been designed for various applications of resonant RF devices such as accelerators or beam deflectors [1], [2]. This report presents compact signal detection algorithms, used in most of developed systems. Application-specific extension of the signal processing procedure allows the system be synchronized to external self-excited oscillator.

SIGNAL AND SYSTEM PARAMETERS

Linear accelerator of charged particles use a resonant principle, where the EM field energy from period to period converted into the energy of accelerated particles. For conversion efficiency, it is important to keep the resonance condition during the system operation cycles. In addition, systems of several resonators need certain and accurate phase difference between oscillations in different resonators. The signal, taken from high-O resonator, occupies narrow frequency range, defined by the resonator characteristic, shown as an example in Fig. 1. Systems with dynamic phase control use a resonator model to build an efficient feedback transfer function. There is always a trade-off between efficiency on one hand, and resource cost of the signal processor on the other. Normally a first order model describe the resonator very well. However, as it is seen in Fig. 1 the difference is visible.



Figure 1: The frequency characteristics of the cavity, 1st order cavity model and overall frequency response of the digital processing unit.

The signal detection needs another compromise. Fig. 1 shows the frequency response of the signal processor. Besides, it shows how ineffective is a resonator as a filtering device. To keep the efficiency the signal processor must reduce the system's sampling rate down to

reasonable low value. For that, it wastes the signal power outside of 500 kHz band.

THE BASE ALGORITHM

Fig. 2 presents the general process used to handle RF signals. The carrier frequency of the RF is higher than the sampling frequency of an ADC or system clock frequency of an FPGA-based digital signal processor (DSP). Because of this the ADC operates in IF mode, working as frequency down converter. The intermediate frequency signal is an input signal for the DSP.



Figure 2: The signal evaluation in the digital domain.

As it is shown in Fig. 2, the first stage of the DSP performs an additional frequency conversion. The system set up defines precisely the frequency shift by a frequency tune word (FTW) of the numerically controlled oscillator NCO. The following low-pass filter suppress image and carrier frequencies existing at the down converter output. The output of the filter is a complex amplitude slowly varying in time. The cost of algorithm is important. To keep the efficiency and effective use of the FPGA resources the data needs to be rarefied according the system bandwidth. Due to the slow signal, the DSP reduces the data rate by factor N, normally down to 1 MSPS. Until this DSP uses a fixed-point arithmetic and Cartesian representation of complex amplitudes. The COordinate Rotation DIgital Computer module converts complex data to the vector form. Then the DSP store the amplitude and phase of the signal in separate buffers.

Fig. 3 gives an example of a system, where the original signal 1 is taken from the master self-excited generator, is used for synchronization of EM-field in the resonator of the novel just designed acceleration section. For successful operation, the digital controller must synchronize two system within 50-microsecond interval after the master-generator start. A distinctive feature of the described system is an oscillation of the amplitude and phase at the rising edge of the reference signal's pulse.



Figure 3: Original signal envelope (1) and some of DSP signals.

Different low-pass filters give different result. A wideband system response, shown as curves 2 in Fig. 3, follows the oscillation of the master-generator. A narrowband system (curve 3) produce smooth signal, but the delay time is critical.

NON-PARAMETRIC METHODS

The algorithm described above uses a continuous data stream to produce a decimated data. There are some situation, which require more detailed signal observation. The system uses a short time interval (shown with marker 4 in Fig. 3) to store a portion of raw data for further offline analysis. The main way of the raw data treatment is a fast Fourier transform.



Figure 4: Raw data and 'momentary' FFT spectrum.

Fig. 4 on top shows captured data and a window function used for sharpening of the spectral lines. As it is seen in the bottom of Fig. 4, even pure sinusoidal signal produces a pattern of spectral lines instead of the single peak. The signal processor uses most significant lines of the pattern to determine final values – phase and amplitude of the signal. The window function smoothly

sew up the data patterns, but also waste some signal strength and produces a phase error (see Fig. 5).



Figure 5: Phase error for the set of window functions.

Fortunately, the phase error due to the window function has only small fraction, depending on phase. Significant frequency dependent phase shift error plays no role due to the relative nature of phase measurements.

PARAMETRIC METHODS

The parametric least squares method used to solve the broadening of the spectrum lines problem. We know that the actual signal is a sin and therefore looking for the most appropriate parameter set of function

$$A_i = \zeta_0 + \zeta_1 * \cos(2 * pi * \zeta_2 * iT_{ADC} + \zeta_3),$$

having minimal power of residual signal:

$$P_{res} = K \sum_{i=1}^{N} (A_i - Y_i)^2,$$

where Y - stored ADC data, K-normalizing factor.

For systems, using a reference generator, the parameter ζ_2 , or reference frequency, is known. The method works well for signals with large signal-to-noise ratio, which is true in considered cases. Fig. 4 shows the spectrum of the residual signal. A sine signal of 2.405 MHz absorbs all energy of the pattern 1. The spectrum of the residual signal is shown in Fig.4.

On the other hand, method is not so good for complicated signals with weak fractions, like the second signal harmonic in Fig. 4. Use of simplex or gradient LSmethods to determine parameters of peak 2 will not give an accurate result in the presence of strong harmonic 1. Other methods are too inefficient to be implemented in front-end electronics.

EXAMPLE. EIGHT-CHANNEL SIGNAL PROCESSOR

Fig. 6 shows a structure of an FPGA-based eightchannel signal processor used in multichannel reference generator with automatic phase control option. In general, Fig. 6 corresponds to Fig. 2. It includes a frequency converter, a three-stage digital decimation filter consisting of two Hogenauer's filters (CICa and CICb) and FIR-filter of 20^{th} order, CORDIC and the data buffer. For better efficiency, the system uses a time multiplexing of data streams. The data rate from the ADC is 4.6(6) times lower than processor's clock, and single decimation filter CICa is able sequentially handle the data from four ADCs. Then the time multiplexer unites all eight channels into one stream to the input of CICb. As a result, the signal processor uses only 20 embedded FPGA DSP blocks. Ten of them are dedicated to the 128-point fast Fourier transform, four used in frequency converters, and five – in FIR filter. The Blackman window-modulator takes the last DSP block.



Figure 6: Eight-channel signal processor.

In addition to the signal processing part the FPGA implements timing and synchronization elements, peripheral control functions and interface to the auxiliary microprocessor including the direct memory access.

CONCLUSION

ITEP has developed a set of RF signal processors for low-level RF applications. The digital core of developed modules provides a great flexibility in signal generation and control. The 'standard' streaming algorithm of the input RF data processing is suitable in most of applications.

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