FAST TUNE MEASUREMENT SYSTEM

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Abstract

Tune measurement system developed in Budker Institute of Nuclear Physics provides fast and accurate measurements of fractional part of betatron tunes in electron-positron storage rings and accelerators.

The tune measurements rate can achieve 1 kHz. It is especially important for electron-positron accelerators to have tunes measurement data for each phase of accelerating cycle.

The developed system is planned to be installed at the NSLS-II Booster Synchrotron. The system can perform up to 330 measurements during 300ms time interval of Booster energy ramping. The kicking technique is used as measurement method. The kicks are carried out by a radio frequency (RF) pulses. Each RF pulse contains two frequencies and thus can simultaneously excite the horizontal and vertical betatron oscillations.

All signal processing including FFT is performed inside FPGA. The tune measurement accuracy is better than 0.0005.

The developed system was put into operation at the February 2011 in VEPP-3 electron-positron storage ring at BINP.

INTRODUCTION

Booster synchrotron for third generation synchrotron light source NSLS II is presently under construction in BNL, USA [1]. The Booster main parameters are given in Table 1.

Table 1: Main parameters of the NSLS II Booster

Beam energy injection/extraction	200 MeV/3 GeV
Repetition rate	1 Hz (2 Hz)
Revolution frequency F_0	1.894 MHz
RF frequency	499.68 MHz
Betatron tunes: ν_x/ν_y	9.6455 / 3.4105
Beam current	1-30 mA
Energy ramping time	300 (150) ms

Requirements to Tune measurement system (TMS) for the Booster synchrotron are:

- Tune measurements rate has to be up to 1 kHz
- Tune measurements accuracy has to be better than 0.5×10^{-3}.

TMS satisfied to these requirements has been designed and fabricated at BINP. The system includes two identical sets of of four 50-Ω striplines and TMS electronics. One set is a Kicker for beam excitation; another one is a Pickup for measurement of a beam response signal.

The system uses the kicking method for tunes measurement. The beam is excited by radio frequency (RF) pulse with the frequency f_e close to $f_B = (1 - \nu_{x,y})f_0$, where f_0 is the revolution frequency, $\nu_{x,y}$ – is the fractional part of the horizontal (vertical) tune. Duration of the RF pulse is 100-200 µs. The measurements are possible when the difference between frequency f_e and betatron frequency $(1 - \nu_{x,y})f_0$ does not exceed $(0.01\text{-}0.02)f_0$. In this case, the signal of the beam betatron oscillations is received by the stripline pickup after the end of the exciting RF pulse. Then the signal is transferred to the signal processing electronics, where it is sampled by ADC and is processed by a Field Programmable Gate Array (FPGA) circuit. The result of signal processing is the values of $\nu_{x,y}$.

SYSTEM STUCTURE

The structure chart of the Tune measurement system is presented in Fig. 1.

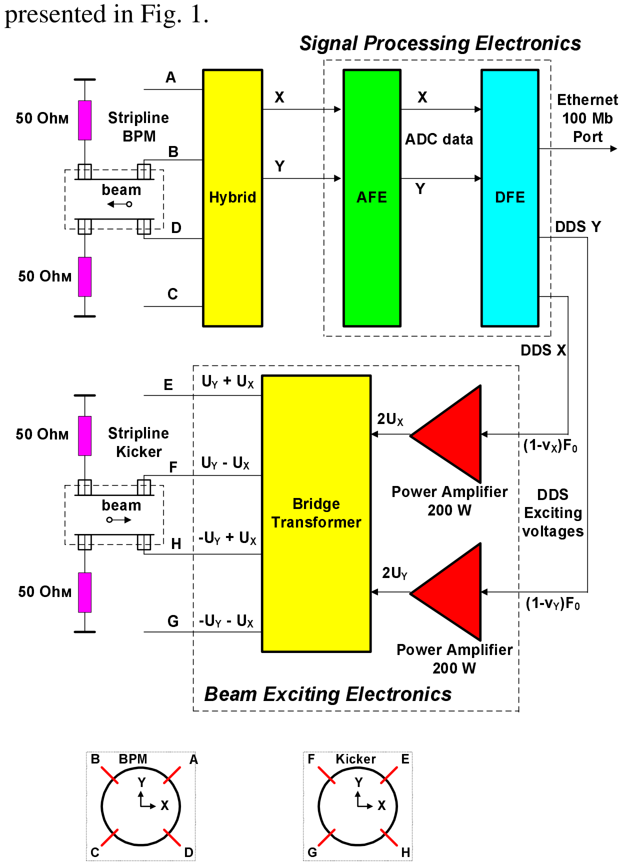

Fig.1. The structure of the Tune measurement system.

The system consists of Pickup, Kicker, Hybrid, Signal Processing Electronics and Beam Exciting Electronics. The Pickup and Kicker stripline electrodes are mounted at

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the angle of 45° relative to the horizontal plane using a BINP-made 50 Ω/450°C vacuum-tight feedthrough for SMA plug with bearing capacity. The length of stripline is 450 mm, which is about 3λ/4 (λ is the wavelength) at RF frequency of 499.68 MHz.The printed circuit Hybrid is placed near the Pickup. The signals proportional to horizontal (X) and vertical (Y) beam oscillations come from Hybrid to Signal Processing electronics which consists of Analog Front End (AFE) Electronics and Digital Front End (DFE) Electronics.

Beam Exciting Electronics consists of two 200 W Power Amplifiers, Bridge transformer and 50 Ω loads. Two RF pulses from DDS synthesizers located in Signal Processing electronics come to the Power Amplifiers (PA) inputs. From PA outputs RF pulses with amplitude up to 140 V are distributed to four kicker striplines by Bridge transformer. Such scheme provides selective or simultaneous excitation of both horizontal and vertical betatron oscillations. Sum power of 400 W allows excite beam oscillations up to 1 mm amplitude in all beam energy range.

SIGNAL PROCESSING ELECTRONICS

Analog Front End (AFE)

A functional diagram of the AFE electronics is presented in Fig.2.

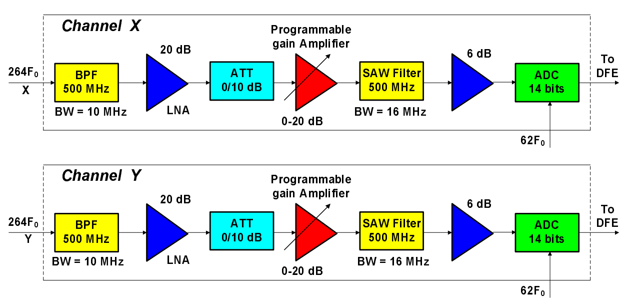

Fig.2. Functional diagram of the AFE electronics.

The Analog Front End consists of two identical processing channels (*X* and *Y*). The first harmonics of RF frequency ($264F_0$) is extracted from the signal spectrum. Input printed-circuit Band Pass Filter has the following parameters:

- central frequency – 500 MHz
- bandwidth – 10 MHz
- insertion loss – 3 dB

After amplification by the Low Noise Amplifier (LNA) HMC616LP3 the signal passes through programmable Attenuator 0/10 dB (HMC541LP3) and programmable Gain Amplifier (PGA). The PGA provides 3 fixed gain values: 0 dB, 10 dB and 20 dB. The second Band Pass Filter (SAW filter TA0979A of Goledge) with bandwidth of 16 MHz minimizes noise and distortions and provides additional suppression of mirror components, thereby providing insensitivity to signal phase. The signals are sampled by 14-bit ADC (AD9246 of Analog Devices) with sampling frequency $f_{ADC} = 62f_0 \approx 117$ MHz. The digitized signals come to the Digital Front End, where they are processed by the FPGA.

Digital Front End (DFE)

Functional diagram of the Digital Front End (DFE) is presented in Fig. 3.

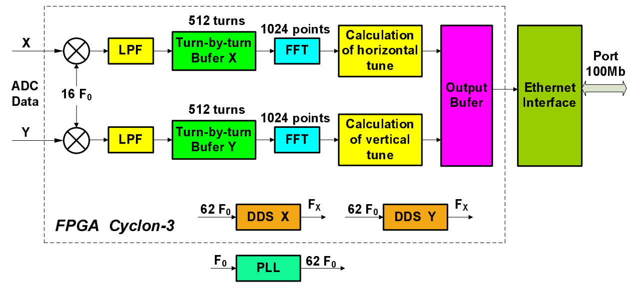

Fig.3. Functional diagram of the DFE.

The core of the DFE is FPGA Cyclon-3 EP3C40 produced by Altera. Due to frequency folding the signal frequency at the FPGA input is $16f_0$. Digital processing performed by the FPGA includes synchronous detecting, filtering and Fast Fourier Transformation (FFT) of the turn-by-turn data array. Before FFT two additional procedures are performed:

1) the average value (signal of orbit displacement) is subtracted from the turn-by-turn data array;
2) the array is multiplied by Hann window.

After 1024-points FFT the spectrum centre of gravity is calculated. This centre of gravity corresponds to the desired betatron tune. The time required for digital signal processing of two signals (X and Y) is about 0.5 ms.

The FPGA also contains two Direct Digital Synthesizers (DDS). Each DDS generate a sinusoidal signal. These 10-bit digital signals come to DACs and then to Power Amplifiers of the Beam Exciting Electronics.

A clock signal for ADCs and FPGA with frequency of $62f_0 \approx 117$ MHz is generated by the low jitter PLL AD9516-4. Measured jitter of this PLL is 0.4-0.5 ps.

Signal Processing electronics occupy two 1U 19” chassis.

MEASUREMENT CYCLE

Time diagram of the measurement cycle is represented in Fig.4.

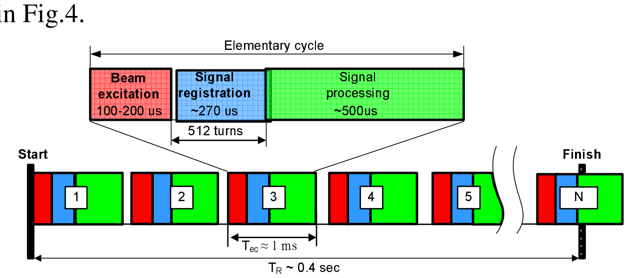

Fig. 4. Time diagram of the whole measurement cycle.

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The whole measurement cycle starts from beginning of the Booster energy ramping and consists of N elementary cycles. Each elementary cycle includes 3 stages: beam excitation, signal registration and signal processing. The total time of one elementary cycle T_{ec} is less than 1 ms. The tune measurement is possible when the difference between DDS frequency and frequency $(1 - \nu_{x,y})f_0$ does not exceed $(0.01\text{-}0.02)f_0$. In this case, the signal of the beam betatron oscillations appears at the end of the exciting RF pulse. If the betatron frequency is not known with accuracy $(0.01\text{-}0.02)f_0$, the search mode is required. In the search mode DDS frequency for elementary cycle n+1 differs from DDS frequency for elementary cycle n in fixed value Δf. So, during the whole measurement cycle DDS frequency is scanning in specified range. For elementary cycle n_0 where DDS frequency is more close to $(1 - \nu_{x,y})f_0$ the signal of betatron oscillations is maximal and betatron frequency is found. Then the measurement mode can be started. In the measurement mode, the DDS frequency tracks to the betatron frequency. DDS frequency for elementary cycle n+1 is set equal to betatron frequency measured during elementary cycle n. The search mode can be used in fixed energy, for example in injection energy. Then before energy ramping DDS frequency is set to $(1 - \nu_{xi,yi})f_0$, where $\nu_{xi,yi}$ is the measured tune at injection energy.

EXPERIMENTAL TESTS RESULTS

Made at BINP TMS electronics had been tested at Lab test stand. Scheme of Lab test is presented in Fig.5.

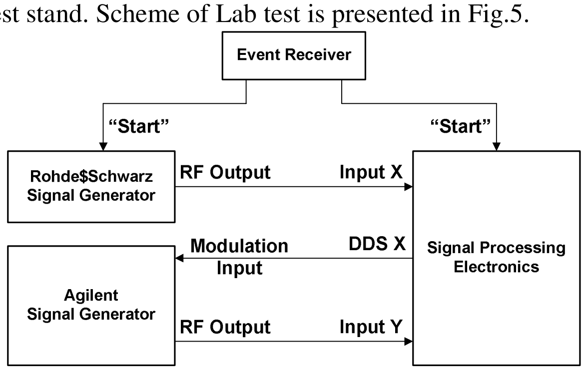

Fig.5. Scheme of Lab test of TMS electronics.

Two RF signal generators are used in this test. The first one (Rohde&Schwarz SMB 100A signal generator) generates sinusoidal signal ~500 MHz, 1mV with amplitude modulation. Amplitude modulation frequency F_{MOD1} is changing linearly in the range $(0.1\text{-}0.2)\ f_0$ during the time 300 ms after "Start" pulse coming from Event Receiver (EVR). The same pulse comes to Signal Processing electronics starting the measurement cycle. Signal Processing electronics measure modulation frequency F_{MOD1}. DDS X frequency F_{DDSX} is tracking to the measured frequency F_{MOD1}. Output of DDS X is connected to the external modulation input of the second RF signal generator (Agilent). So, at the Agilent output we have ~500 MHz, 1mV sinusoidal signal with F_{DDSX} amplitude modulation. This signal comes to the Input Y of the Signal Processing electronics. Difference between two measured frequencies F_X and F_Y gives the measurement error. This test gives tune measurement error does not exceed 10^{-4}.

Analogues TMS electronics has been installed at BINP storage ring VEPP-3. The difference between the systems is tied mainly with another VEPP-3 RF frequency – 72.54 MHz. The second harmonics of RF frequency is used in the Signal Processing Electronics. Results of tune measurements with beam at VEPP-3 (beam energy is ~1.8 GeV) are represented in Fig.6.

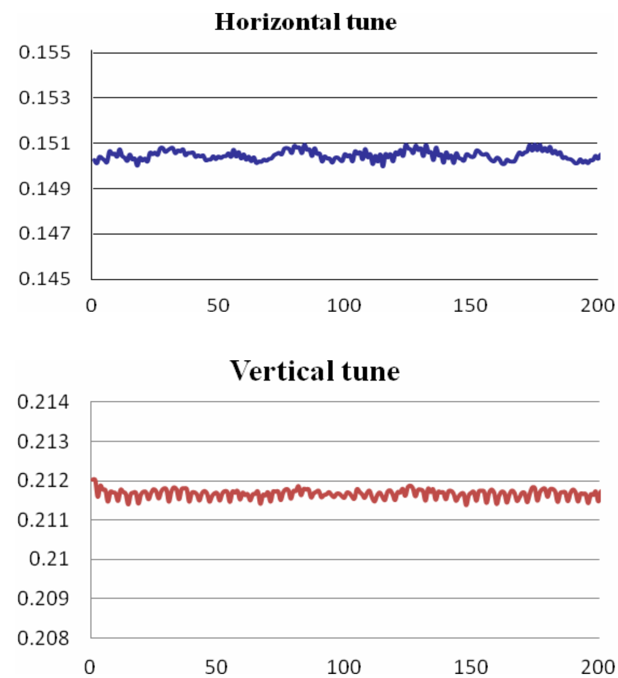

Fig.6. Results of horizontal (upper) and vertical (lower) tune measurements with beam at VEPP-3 at ~1.8 GeV.

Beam oscillation amplitude was about 200 microns. Root-mean-square deviation of measured betatron frequencies σ is 3×10^{-4} for horizontal plane and 2×10^{-4} for vertical plane. Such relatively large σ can be caused by real instability of the betatron frequencies at VEPP-3.

SUMMARY

Developed at BINP Tune Measurement System satisfies all requirements of NSLS-II Booster. At present all TMS components have been manufactured and tested. It is planned at the beginning of 2013 the system will be commissioned at BNL. Analogues TMS successfully works in VEPP-3 storage ring at BINP since February 2011.

REFERENCES

[1] S. Gurov at al/ STATUS OF NSLS-II BOOSTER // PAC'11 New York, NY, USA, WEP201, p1864.

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