IMPLEMENTING ELEMENTS OF DIGITAL TRANSVERSE FEEDBACK SYSTEM IN ALTERA FPGA.

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Abstract

The transverse feedback system is intended to damp beam position errors after injection into an accelerator and cure beam instabilities during acceleration. The system consists of pick-ups, low level electronics making necessary signal processing and power electronics. Implementation of the low level electronics elements in Altera StratixII DSP development kit is described. The realized digital signal processing allows keeping an optimal phase between pick-up and kicker with changes of revolution frequency during accelerating cycle.

INTRODUCTION

The transverse feedback system is intended for damping of beam oscillations due to injection kicker ripple and stabilization of a beam against coupled bunch transverse instabilities.

The typical digital transversal feedback system schematic diagram is shown on the Figure 1.

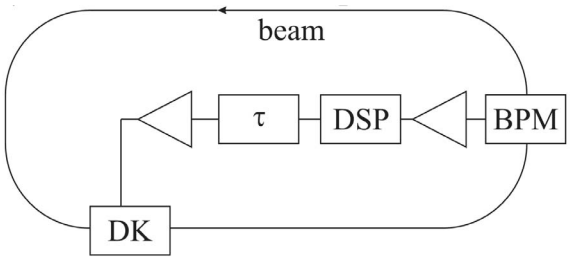

Figure 1: Digital transversal feedback schematic diagram.

The beam displacement signal measured by beam position monitor (BPM) is amplified, converted to digital form, processed by digital signal processing (DSP) circuit, delayed to match signal transition time from BPM to deflector (DK) with beam flight time, converted back to analog form, amplified and applied to the beam by means of deflector. To obtain the optimal damping, the phase advance between BPM and DK have to be odd multiplies of π/2.

HARDWARE

Altera Sratix II EP2S60 DSP development board was used for digital processing and control unit implementation. The core of the board is Stratix II EP2S60F1020 device, which provides more then 60,000 equivalent logic elements (LEs), up to 2.5 Mbits of internal memory arranged in TriMatrix memory blocks, operating at up to 450 MHz. The device also contains 12 enhanced/fast phase-locked loops (PLLs) and 36 DSP blocks, giving 144 18x18bit multipliers.

Analog I/O of the board includes two 12-bit 125-MHz ADCs and two 14-bit 165-MHz DACs from Analog Devices.

The board has set of the external memories, including 32Mbytes of SDRAM, 1MByte of SRAM, 16 Mbytes of flash memory.

The digital I/O contains RS-232 serial port and 10/100 Ethernet physical layer/media access control (PHY/MAC).

The rich set of the development board and FPGA features allows implementing both digital processing and controlling program, so the complete digital transversal feedback can be realized in the one board. The system can be controlled via Ethernet from external PC or control system.

Digital processing and control parts of the system are described below.

DSP: OVERVIEW

The block diagram of the digital signal processing, realized in Stratix II FPGA is presented on the Figure 2.

Two BPMs separated by quarter betatron wave length are used to implement so called 'virtual pick-up', which has a correct betatron phase advance relative to the deflector position. The difference signals from two BPMs are digitized by 12-bit ADCs, signal from the first BPM needs to be delayed by time of flight between BPMs.

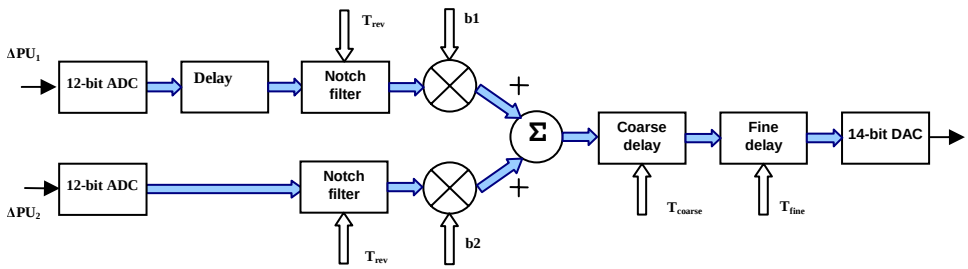

Figure 2: Block diagram of the digital signal processing part.

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Notch filters reject closed-orbit offset signal at revolution harmonics. After that, signals are mixed with coefficients b1 and b2 coming from trigonometric expression

$$\cos(\omega t - \varphi) = \cos\omega t \cdot \cos\varphi + \sin\omega t \cdot \sin\varphi .$$

The resulting signal has to be delayed to apply deflector action on the same particles that generated the BPM signals and compensate the fixed delays in electronics and cables, so $T_{coarse} + T_{fine} + T_{fix} = T_{flight}$. The value of the overall delay is usually less than one turn revolution period.

In case of variable revolution frequency, it is necessary to calculate and make adjustments of the notch filters rejection frequency and all delays values during the accelerating cycle. Either external analog signal of RF frequency or digital code from external control system can be used to obtain the revolution period value.

DSP: COARSE DELAY

Coarse delay is implemented as dual port memory clocked with the clock frequency of the board allowing making the delay with 10ns step.

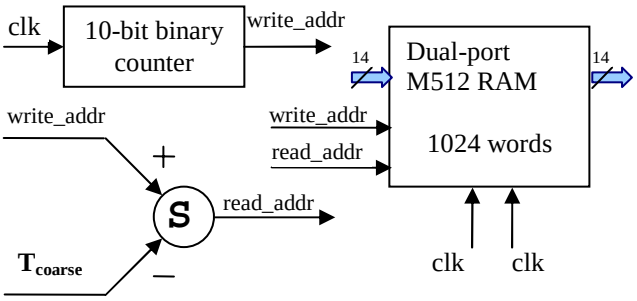

Figure 3: Coarse delay implementation

The data is stored in 1024 bit dual port memory, the read and write clocks are the same. The address of RAM cell to write the data is calculated by 10-bit binary counter, which value is incremented every clock period until it reaches 1023 after which the counter starts to count from zero. The address of RAM to read data from is calculated by subtraction of the necessary number of clock cycles from write address.

The size of the memory and clock frequency defines the maximum delay that can be achieved. The EP2S60F1020 device has more than 2.5 Mbits of internal memory allowing to implement up to 2ms delay for the 12bit data with the master clock frequency of 100MHz.

DSP: FINE DELAY

Fine delay is implemented using internal FPGA resources such as PLL (phase locked loop). EP2S60F1020 device contains 12 PLLs which can be used to produce phase shift of the clock allowing delaying data for specified amount of time. The minimum delay step depends on the frequency of the PLLs voltage controlled oscillator (VCO) and is equal to the 1/8th of its period allowing to achieve 125ps resolution. PLL can be reconfigured in real time allowing adjusting output clock phase on the fly.

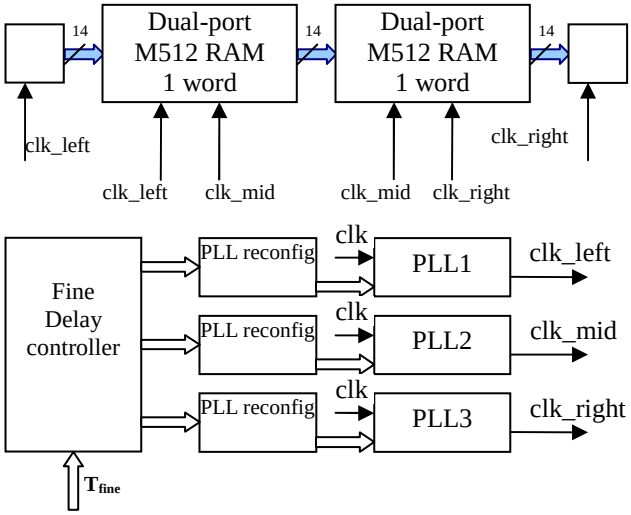

Figure 4: Fine delay implementation

Clock domains transfer is organized using two M512 dual-port memory blocks with individual clocks for writing and reading. The date is written and read from the same RAM cell but with different clocks shifted by phase. Thus the total amount of phase shift can be made up to 10ns while the phase shift between neighbor memory blocks is up to 5ns.

The phase response of the board when switching between 0 and 25ns delay (-9° phase shift at 1MHz) is shown on the Figure 5. 20 ns of the delay are implemented by coarse delay module and remaining 5ns by fine delay module.

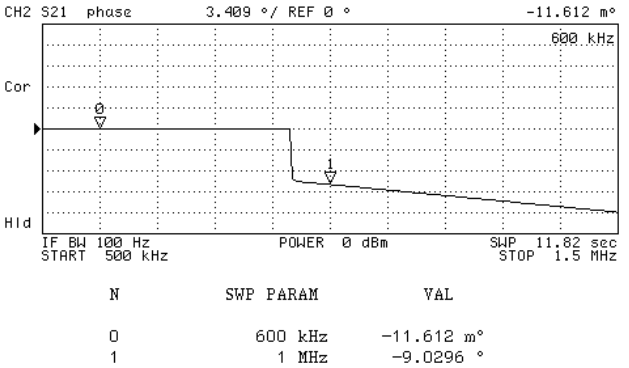

Figure 5: Phase response with 25ns digital delay

DSP: NOTCH FILTER.

The notch filter consists of the one-turn delay and synchronous adder (see Figure 6). One-turn delay is implemented the same way as the coarse delay described above.

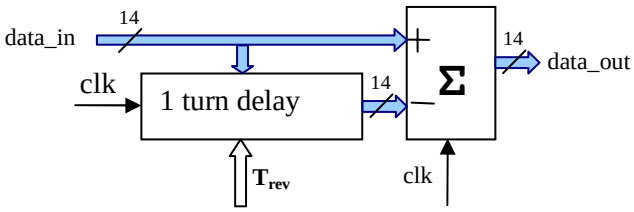

Figure 6: Notch filter implementation

The notch filter frequency response is shown on Figure 7 (revolution frequency is 2MHz on this picture). It can be seen that the filter blocks signal with multiples of the revolution frequency. Gain and produced phase shift depend on the frequency and have to be taken into account.

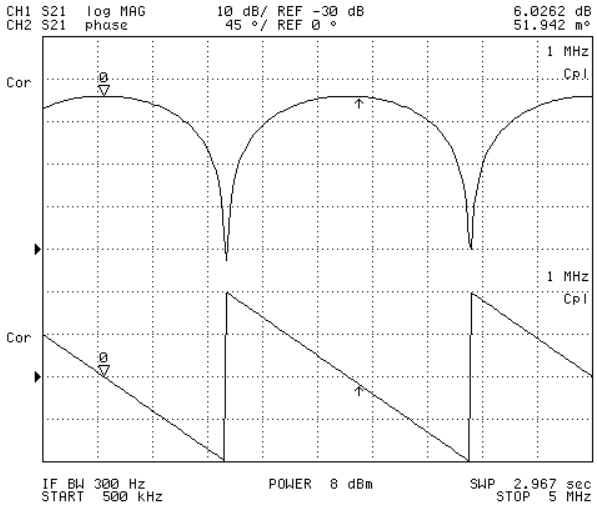

Figure 7: Notch filter gain and phase response.

CONTROL: OVERVIEW

The main task for the control is to communicate with external control system, recalculate coefficients and delays according to revolution frequency and update DSP part of the system.

The embedded NIOSII processor was used to fulfill this task. The processor is implemented in the same FPGA and using part of its resources as well as external board resources such as 1Mbyte SRAM memory, 16Mbytes flash memory and 10/100 PHY/MAC Ethernet controller (see Figure 8).

The processor runs real time operating system (RTOS) µC/OS-II, which executes two tasks – InterNiche TCP/IP stack and control application which calculates the DSP coefficients using information received from network. The interface between application and DSP part of the FPGA is carried out by memory mapped I/O ports.

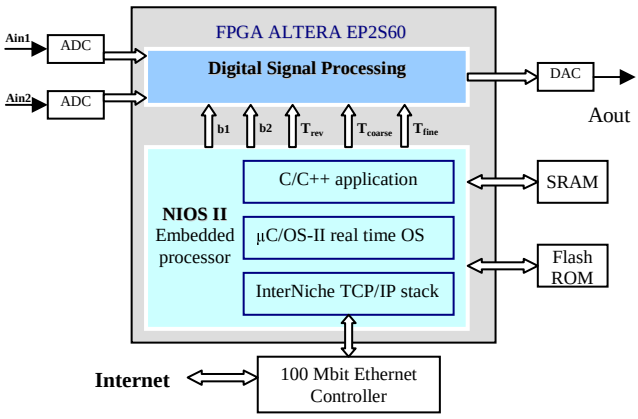

Figure 8: System layout

The external PC control program is written in LabView system (see Figure 9). It allows communicating with the board, setting the revolution frequency and delay, enabling or disabling individual DSP elements.

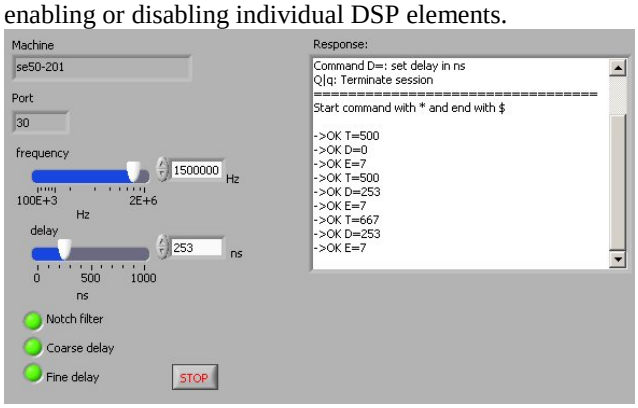

Figure 9: LabView control program

CONCLUSION

Full prototype of the digital transversal feedback system was implemented in Altera Stratix II DSP board including:

- DSP electronics with automatically adjustable notch filter, coarse and fine delays (VHDL/schematics).
- The control system with use of embedded processor NIOSII, uC/OS-II real-time operating system and custom C/C++ application.
- The LabView program for PC to manage the board over Internet.

The feature of the system is implementation of the DSP and control parts in the same FPGA. It allows setting up simulations of the feedback with calculated beam response.

REFERENCES

[1] E. Gorbatchev et al. “Transverse Damping System at SIS100”, EPAC 2006, Edinburgh, June 2006, p. 3014

[2] V. Rossi, “Digital Signal processing and implementation for accelerators”, CERN-SL-2002-047