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DESIGN AND IMPLEMENTATION OF FPGA BASED PROTECTION SYSTEM FOR BEAM ACCELERATION IN LINEAR IFMIF PROTOTYPE ACCELERATOR

Y. Hirata†, A. Kasugai, National Inst. for Quantum and Radiological Sci. and Technology, Rokkasho, Japan
H. Takahashi, Japan Atomic Energy Agency, 319-1195 Tokai, Japan
A. Marqueta, A. Jokinnen, Fusion for Energy, 039-3212 Rokkasho, Japan

Abstract

The IFMIF (International Fusion Materials Irradiation Facility) Prototype Accelerator (LIPAc) has been developed in the Engineering Validation and Engineering Design Activity (EVEDA) phase. The LIPAc is designed to produce a deuteron CW beam with a current and an energy of 125 mA and 9 MeV. After the injector campaign, the LIPAc is entering the RFQ (Radio-Frequency Quadrupole) commissioning phase in which such subsystems as the RFQ, RF system and Beam Instrumentation systems have been attached.

The LIPAc control system consists of local control systems (LCSs) and the central control system. The LCSs haven been developed by Europe and delivered with the subsystems; and the central control system, including personnel and machine protection, timing, archiving and alarming, has been developed by Japan. Japan and EU are jointly integrating them to control the whole accelerator in an organized manner.

Fabrication of the control system is made on the EPICs platform to reduce the risk in integration. Some part of the protection systems has been implemented in FPGA to satisfy both the speed and sophisticated control. The basic idea and implementation of the control system will be presented.

INTRODUCTION

The IFMIF Prototype Accelerator has been developed in the Engineering Validation and Engineering Design Activity phase. The final target of the LIPAc is to generate a heavy deuteron CW beam with a high intensity and 125 mA and an energy of 9 MeV for an average power of 1.125MW.

The control system of the LIPAc consists of six subsystems: Central Control System (CCS), Local Area Network (LAN), Personnel Protection System (PPS), Equipment Protection System (MPS), Timing System (TS), and Local Control System (LCS) of subsystems. Europe and Japan have been developing the control system jointly, in which Europe is in charge of LCSs and Japan five other systems. Upon completion of the implementation, the LIPAc is planned to be operated from the CCS and the operational parameters and experimental data can be monitored from the CCS and archived by the archive system.

After the completion of the injector campaign (Phase A), the RFQ, RF system, LLRF, MEBT and BI (beam instrumentation systems) are being attached to the injector (Fig. 1) and the development of the LIPAc has entered the RFQ commissioning phase (Phase B) [1].

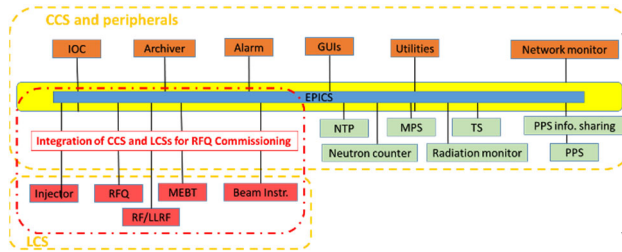

Figure 1: Control system configuration for RFQ commissioning.

PPS and MPS have an aspect of final protection scheme. Parameters such as thresholds, etc., are not supposed to be changed once they are determined. So, they are implemented basically using PLC-based technology for the general slow interlocks. For faster interlocks, such custom-made cards as those with Application-Specific Integrated Circuits (ASICs) have been needed when both speed and reliability are mandatory.

In recent years, an architecture using FPGA is frequently used to achieve both time performance and reliability with more flexibility. As the logic required some systems are more complicated, FPGA is advantageous in faster development, adaptability, reusability and therefore reduced final costs.

In such a case as IFMIF, subsystems are developed and delivered by different countries and detail specs are not fully prepared/agreed in advance, since some interlock conditions and their criteria could be complicated and likely determined from experiments. From these reasons some part of the LIPAc protection system uses an FPGA architecture.

In this workshop, the authors will present cases of such inter locks as chopper [2], beam counting and overload protection for diagnostics system used in LIPAc.

CHOPPER INTERLOCK

A chopper is used to allow interceptive diagnostics after the RFQ. Due to the high power and long rise time of the beam extracted from the ion source, pulsed mode operation is used (Fig. 2) to prevent damage on the diagnostics. A high voltage is applied to the chopper which deflects the beam usually. In response to the timing sig-

† hirata.yosuke@qst.go.jp

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nal, the voltage applied to the chopper turns off to pass the beam toward the RFQ. The beam is trimmed or "chopped" to generate a sharper pulse (Fig. 2).

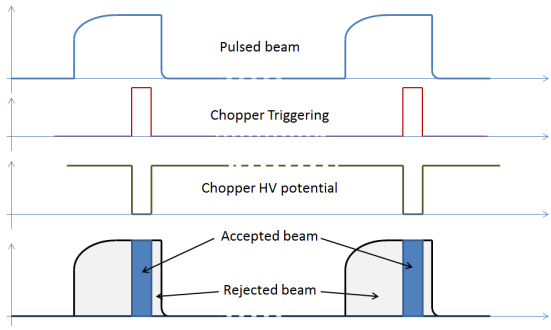

Figure 2: Beam chopping image to create a sharper pulse.

The operation of the chopper is interlocked with several conditions, meaning that the CIM needs to interface with different systems to ensure correct operation. Due to this complexity and trial-and-errors anticipated in the development phase, an architecture using FPGA based on RIO hardware from National Instruments [2] has been adopted.

At the time of development of the Chopper Interlock Module (CIM), LIPAc was already running in the injector commissioning phase. The CIM had to be integrated with the control system (based on EPICS) and other subsystems without interference. Consequently, the CIM was designed to have “armed” status before operation rather than an always-on system.

The first purpose of the chopper is to generate precise pulse lengths prevent overload to the downstream diagnostics, etc. When the CIM is armed, it oversees the chopper triggering gate pulse and takes proper actions depending on the status of the gate signal: gate signal off, gate-on rising, gate-on and gate-off falling. The transition and major actions on each status are summarized in Fig. 3. It should be noted that in this figure non-mentioned status signals from PLCs, etc., are assumed all correct.

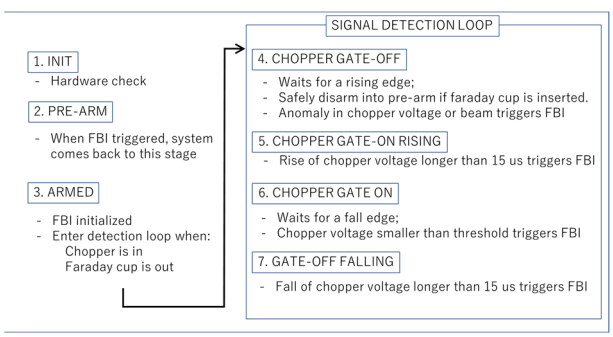

Figure 3: Transition and actions of CIM.

Table 1 summarizes the hardware with major specifications that was selected to meet the requirements for the project. Figure 4 shows the system hardware, together with the signals that the CIM must monitor. The NI CRIO-9068 chassis hosts a microcontroller running a Real-Time Linux. This allows the use of NI EPICS Channel Access (CA) Client and Server so the CIM should be successfully integrated into the LIPAc control system.

The acquired data is transmitted to the LabVIEW RT host and updated on the EPICS Process Variables. The implementation in LabVIEW is a two-stage loop performing read operations and then writing configurable parameters such as thresholds to the FPGA. These configuration parameters will be used in pre-armed state at the beginning of the interlock operation.

Table 1: RIO Components Used in CIM

HARDWARE	PURPOSE
NI cRIO-9068	CompactRIO chassis with embedded controller and 8 slots for modules. FPGA for the interlock, and dual-core CPU for EPICS integration.
NI-9223	Microsecond [-10,+10V] analog 16-bit input module for the High Voltage and ACCT readings. Conditioned by a voltage divider.
NI-9401	High-speed configurable I/O digital TTL module. Configured as a read module to interface with the timing system.
NI-9422	24V industrial logic level input sinking module. This reads signals from the PLC interlocks.
NI-9474	24V industrial logic level output sourcing module. This module drives the signal FBI to low level in the case of an interlock action.

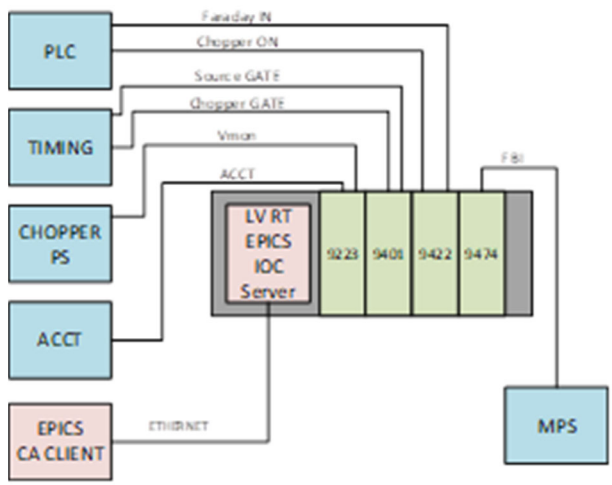

Figure 4: Hardware constitution of CIM.

The solution based on the EPICS CA Client and Server provides a useful mechanism that monitors CIM variables. However, there is limitation in this scheme such that the closed solution does not provide any configuration of the EPICS records and improving this could be a next issue for the extension of FPGA use in the protection systems.

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OVERLOAD DETECTION FOR BEAM INSTRUMENTATION

Several interceptive devices such as SEM grid are installed to examine the beam quality. SEM grid uses thin wires with which the beam profile or other parameters can be measured. While measurement, the beam continues to deposit energy and cause damage on the wire.

The overload detector monitors the beam current, caluculate the deposit energy accumulated on the wire and stops the beam once the acuumulated energy exceeds certain values. These thresholds, however, vary depending on various conditions : beam current and size especially, other than the statuses of other devices.

The SEM grid devlopement group carried out thermal simulation and provided maximum beam length allowed as functions of beam current and size. We simplified these conditions and implemented in FPGA (XC7A100T-1FTG256C) with VHDL as a core part of the overload detector. The simplified contiditions are summarized in Table 2. Other conditions such as statuses of other systems—FC, chopper, beam direction—are considered by the software.

Table 2: Maximum Beam Length Acceptable

	$\sigma_{beam} \leq 10.5$ [mm]	$\sigma_{beam} \geq 10.5$ [mm]
I_{beam} = 0~3 [mA]	$247.78 \cdot \frac{{\sigma_{beam}}^2}{15}$	$247.78 \cdot \frac{110}{I_{beam}}$
I_{beam} = 3~15 [mA]	$247.78 \cdot \frac{{\sigma_{beam}}^2}{15}$	$247.78 \cdot \frac{110}{I_{beam}}$
I_{beam} = 15~125 [mA]	$247.78 \cdot \frac{{\sigma_{beam}}^2}{I_{beam}}$	$247.78 \cdot \frac{110}{I_{beam}}$
$I_{beam} \geq 125$ [mA]	$247.78 \cdot \frac{{\sigma_{beam}}^2}{I_{beam}}$	$247.78 \cdot \frac{110}{I_{beam}}$

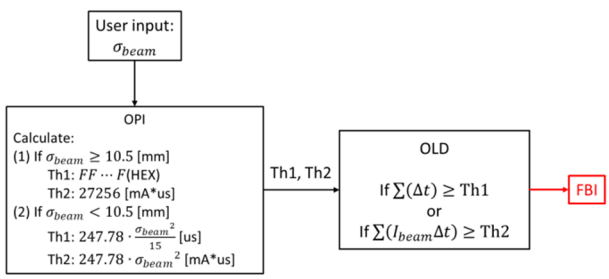

Figure 5: Basic logic of core OLD.

The beam size, which is an input parameter and given by the operator, should be inferred or guessed since it is not precisely known before using the SEM grid. Based on the formulae in Table 2, two threshold values for maximum beam length are calculated in the OPIs and transferred to the FPGA (Fig. 5). The judge as to whether the accumulated current exceeds the threshold is made within the FPGA.

Figure 6 shows the condition of interlock triggering for a beam size of 8 mm. The boundaries are the conditions of Table 2. And if the beam accumulated count exceeds one of the thresholds, the detector triggers an interlock.

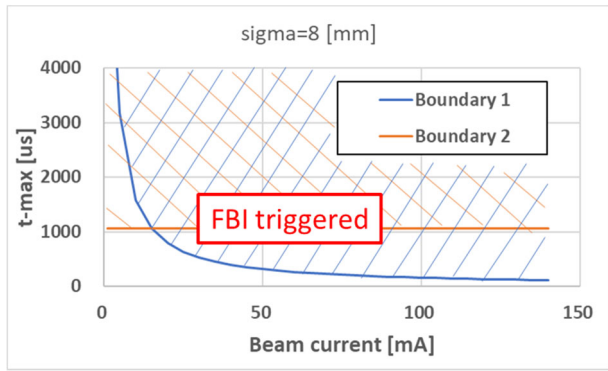

Figure 6: Condition of interlock triggering.

These conditions are complicated and subject to change according to the measurement results. Table 2 could be improved while performing measurements.

SUMMARY

As the development of control systems has been carried out separately in Europe and Japan, a flexible approach is necessary for the protection system to allow effective development. The examples presented in this report shows, the use of FPGA in some complicated conditions is effective in development flexibility in addition to its transaction speed and reliability.

ACKNOWLEDGEMENT

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