THDAPLCO01

EMBEDDED CONTROL SYSTEM FOR PROGRAMMABLE MULTI-PURPOSE INSTRUMENTS

Acknowledgements:
J. Avila-Abellan, S. Blanch-Torné, G. Cuní, D. Fernández-Carreiras, O.Matilla, J. Moldes, M. Rodríguez, S. Rubio-Manrique, J. Salabert, X. Serra-Gallifa, A. Milán, Peter Sjöblom

Agenda

Project Concept

Electronic design

Software Project

Conclusions

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Conclusions

ALBA is a 3rd generation Synchrotron Light facility located in Cerdanyola del Vallès, (Barcelona), being the newest source in the Mediterranean area.

ALBA has a 3 GeV electron beam energy. It currently has eight operational beamlines, comprising soft and hard X-rays, which are devoted mainly to biosciences, condensed matter. There are two beamlines in construction (low-energy ultra-high-resolution angular photoemission for complex materials and microfocus for macromolecular crystallography).

https://www.cells.es/en

Product concept

- ALBA developed years ago a 4 independent channel electrometer
  - To measure from various sources of different nature and magnitude synchronously, while remaining flexible at the same time
- Overall performance is very good but minor changes are needed
- Em# arises to solve that few limitations and provide new functionalities to make it more versatile and customizable.
  - Use of standard interfaces to interconnect devices
  - Increase performance of ADC
  - Use an open-hardware (OHWR) FPGA board
    - Big community of OHWR developers, where to collaborate
  - Control application in a Single board computer(SBC)
- Open collaboration between institutes: ALBA, MAX-IV,…

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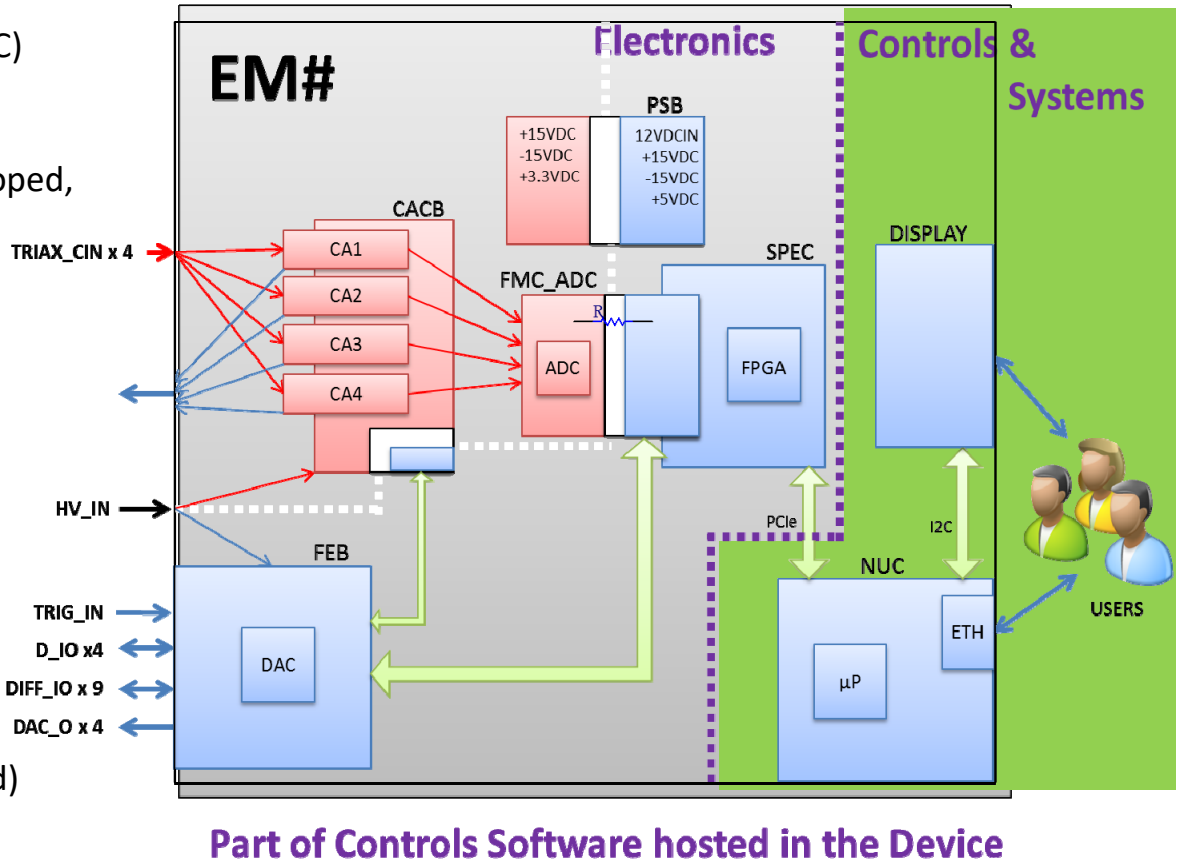
General Block Diagram

The hardware of the equipment is composed by the following boards:

- Simple PCI Express FMC Carrier (SPEC) (commercial, OHL)
- FPGA Mezzanine Card (FMC) (developed, OHL)
- Single Board Computer (SBC): Intel NUC DE3815TYBE (commercial)
- Front-End Board (FE) (developed)
- 4x ALBA Current amplifier (CAX) (modified)
- Current Amplifier Carrier Board (CACB)(developed)
- Power Supply Board (PSB)(developed)
- Display (commercial)



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Software Design

Involves to three software projects all together distributed in a single package

- The Operating System:
  - LINUX: It's Customizable, Open Source, Free, Fast, Secure, Well-Supported…
- The gateware (FPGA software)
  - High performance and fast data acquisition
- The main control software in the SBC (ALIN)
  - Manage different operations to control the Em# reducing the FPGA SW load & complexity
  - Standard, easy to develop, flexible and have a big performance

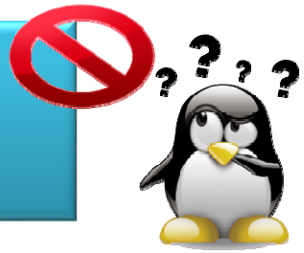
1. Linux OS

Which LINUX distribution?

Pre-built Binary Linux Distributions (Debian, SUSE,..)

+ Readily available
- Large, usually 100+MB
- Not available for all architectures
- Not easy to customize
- Generally require native compilation

Manual System building



+Smaller and flexible
- Very hard to handle cross-compilation and dependencies
- Not reproducible
- No benefit from other people's work

Embedded Linux Build systems

+ Small and flexible
+ Reproducible, handles cross-compilation and dependencies
+ Available for virtually all architectures
- One tool to learn
- Build time

Wide range of solutions: Yocto, PTXdist, Buildroot, LTIB, OpenBricks, OpenWRT...

YOCTO

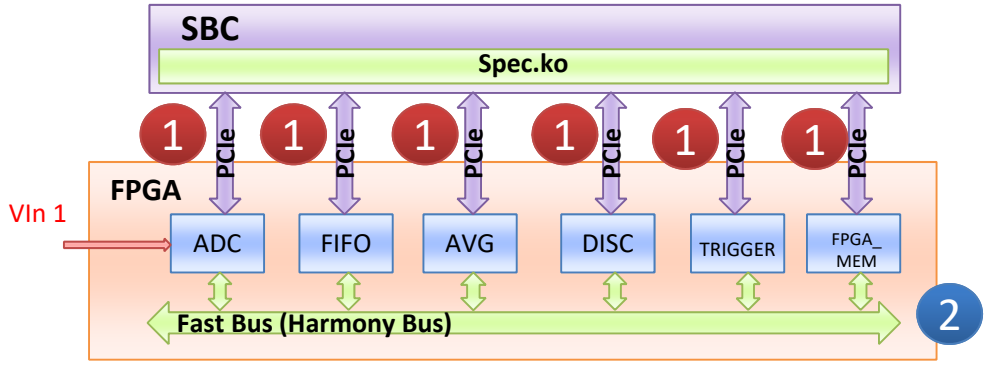
- Builds a complete Linux distribution with binary packages.
- Powerful, and although it is complex and quite steep learning curve, it is quite flexible and offers a high rate of configurability
- Easy to combine it with a SVN, GIT, ...

2. Gateware

High performance and fast data acquisition

- Main software in SBC is not fast enough to get and process the acquisition data at 400KSamples/Second for the 4 channels via PCI.
- Acquisition through the fast acquisition bus: Harmony.

X. Serra, et al., "A Generic Fpga Based Solution for Flexible Feedback Systems", ALBA-CELLS Synchrotron, FRFMPLCO06, PCaPAC 2016



1 Slow bus:
- Direct read of the FPGA blocks
- Use of the SDB structure
- Register map in external files auto-generated

2 Fast bus (Harmony):
- Use of dynamic ID's.
- The SBC configures the ID's using the slow bus
- FPGA stores data in the memory using the Fast Bus with ID and timestamp.

3- Main control software – ALIN (1/7)

Main considerations:

- Possibility to add new functionality /requirements easily.
- Use of the Self Describing Bus (SDB) structure to access the FPGA data.
- Easy integration in any control system: ASCII commands following the Standard Commands for Programmable Instruments (SCPI).
- Local control through a touch-screen display

3. Main control software – ALIN (2/7)

Self Describing Bus (SDB)

OPEN HARDWARE REPOSITORY

- Developed by CERN OHR group. http://www.ohwr.org/
- Allows to enumerate the cores that are available in the current FPGA binary
- It is a self description structure that provides metadata about the logic blocks.
- Each block is assigned to a virtual memory address and its contents is defined in the FPGA code (configuration parameters or data).

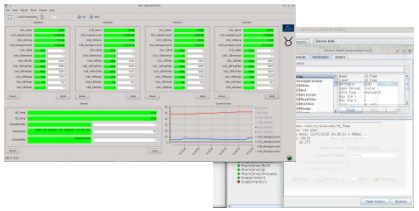
```
~ # alin
#       BusPath VendorId        Product         Address range(hex)      Description
0       0.0     0000000000000651:e6a542c9       0x0L-0x7fffL            WB4-Crossbar-GSI
1       0.1     000000000000ce42:00000601       0x1000L-0x103fL         WB-DMA.Control
2       0.2     000000000000ce42:779c5443       0x1100L-0x11ffL         WB-OneWire-Master
3       0.3     000000000000ce42:00000603       0x1200L-0x121fL         WB-SPEC-CSR
4       0.4     000000000000ce42:00000013       0x1300L-0x13ffL         WB-VIC-Int.Control
5       0.5     000000000000ce42:d5735ab4       0x1400L-0x140fL         WB-DMA.EIC
6       0.6     000000000000a1ba:0000fd11       0x1500L-0x150bL         WB-HRMY-CROSSBAR
7       0.7     0000000000000651:eef0b198       0x2000L-0x3fffL         WB4-Bridge-GSI
8       0.8     0000000000000651:eef0b198       0x4000L-0x5fffL         WB4-Bridge-GSI
9       0.9     ..<< Repository-url >>..        ..........              https://gitcomputing.cells.es/electronics/em2.git
10      0.10    ....<< Synthesis >>.....        ..........              spec_top_fmc_adc
11      0.11    000000000000a1ba:f0884024       ..........              spec_fmcadc400k18b
12      1.0     0000000000000651:e6a542c9       0x2000L-0x3fffL         WB4-Crossbar-GSI
13      1.1     000000000000a1ba:0000fd11       0x3000L-0x300bL         WB-HRMY-CROSSBAR
14      1.2     000000000000ce42:123c5443       0x3100L-0x31ffL         WB-I2C-Master
15      1.3     000000000000a1ba:00000608       0x3200L-0x3230L         WB-FMC-ADC-Core
16      1.4     000000000000a1ba:7565c07b       0x3300L-0x3307L         WB-FMC-FV-CONTROL
17      1.5     000000000000a1ba:00000609       0x3400L-0x340fL         WB-FMC-EM2-SPI-CORE
18      1.6     000000000000a1ba:10856d31       0x3500L-0x353bL         WB-EM2-DIGITAL_IO
19      1.7     000000000000a1ba:9eb04e14       0x3600L-0x360fL         EM2_DAC
20      2.0     0000000000000651:e6a542c9       0x4000L-0x5fffL         WB4-Crossbar-GSI
21      2.1     000000000000a1ba:0000fd11       0x5000L-0x500bL         WB-HRMY-CROSSBAR
22      2.2     000000000000a1ba:0000fdaf       0x5100L-0x510fL         WB-HRMY-ID-GEN
23      2.3     000000000000a1ba:0000f609       0x5200L-0x520fL         WB-HRMY-MEMORY
24      2.4     000000000000a1ba:efea35a4       0x5300L-0x5307L         WB-HRMY-FIFO
25      2.5     000000000000a1ba:efea35a4       0x5350L-0x5357L         WB-HRMY-FIFO
26      2.6     000000000000a1ba:efea35a4       0x5400L-0x5407L         WB-HRMY-FIFO
27      2.7     000000000000a1ba:efea35a4       0x5450L-0x5457L         WB-HRMY-FIFO
28      2.8     000000000000a1ba:b379b5a4       0x5500L-0x550fL         WB-HRMY-AVERAGE
29      2.9     000000000000a1ba:b379b5a4       0x5550L-0x555fL         WB-HRMY-AVERAGE
30      2.10    000000000000a1ba:b379b5a4       0x5600L-0x560fL         WB-HRMY-AVERAGE
31      2.11    000000000000a1ba:b379b5a4       0x5650L-0x565fL         WB-HRMY-AVERAGE
```

```
BaseAdress:             0x2000L
BusPath level:          1.3
Record type             Device Record
ABI class               0x00: 00 00
ABI version major       0x04: 01
ABI version minor       0x06: 01
Bus-specific field      0x07: 00 00 00 04
First address           0x08: 00 00 00 00 00 00 12 00
Last address            0x10: 00 00 00 00 00 00 12 30
Vendor                  0x18: 00 00 00 00 00 00 a1 ba
Device                  0x20: 00 00 06 08
Version                 0x24: 00 00 00 03
Date                    0x28: 20 16 02 24
Name                    0x2c: WB-FMC-ADC-Core
Record Type             0x3f: 0x1L
```

3. Main control software – ALIN (3/7)

Software architecture in SBC

Users



TANGO EPICS

OS LINUX

Applications

Simple applications to control the EM.
- Locally via the Display or the Touch panel
- Remotely via list of functions through remote telnet console (ASCII)

Middleware

Communication protocols or main EM Functions , Diagnostics , Display control, Webserver, Touch control, Others…

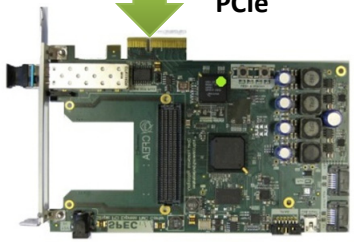
Drivers

Software code of drivers that control physical devices like SPEC, FMC, TCP/IP, Serial, Display, FPGA,SCPI…

USB/Serial

I2C

PCIe

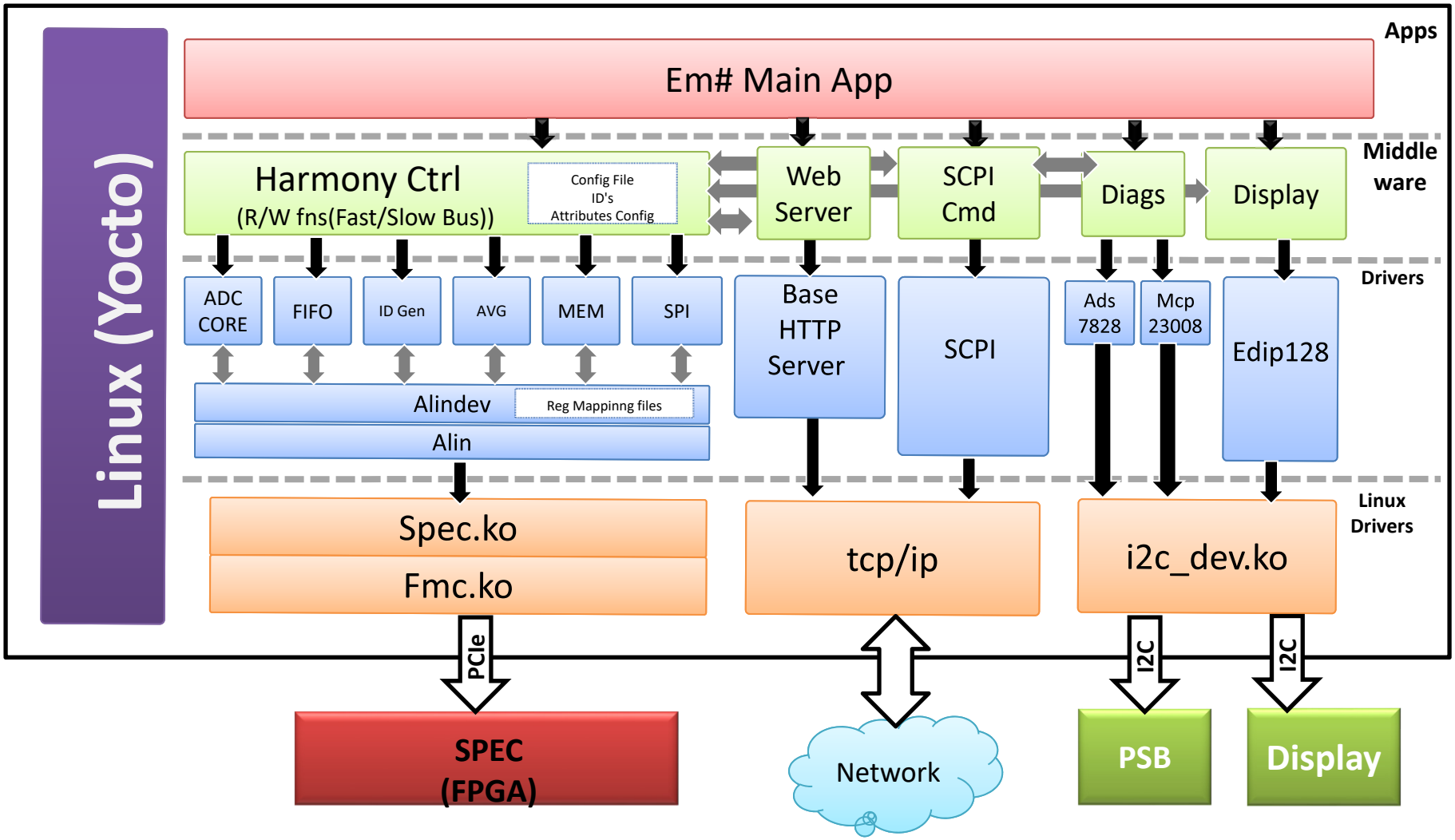


TCP/IP

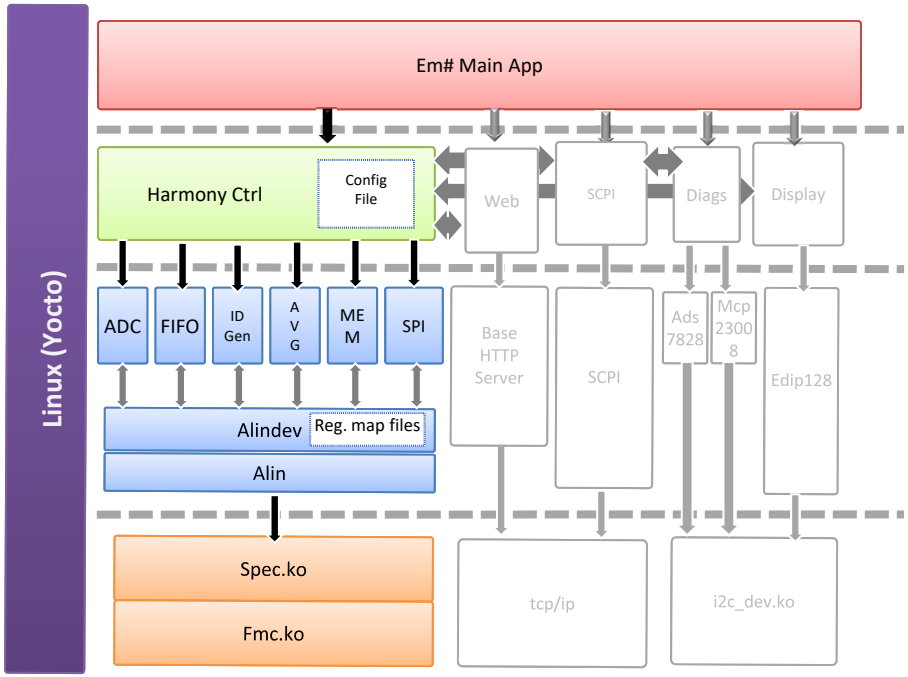
Hardware

3. Main control software – ALIN (4/7)

Software architecture in detail



3. Main control software – ALIN (5/7)

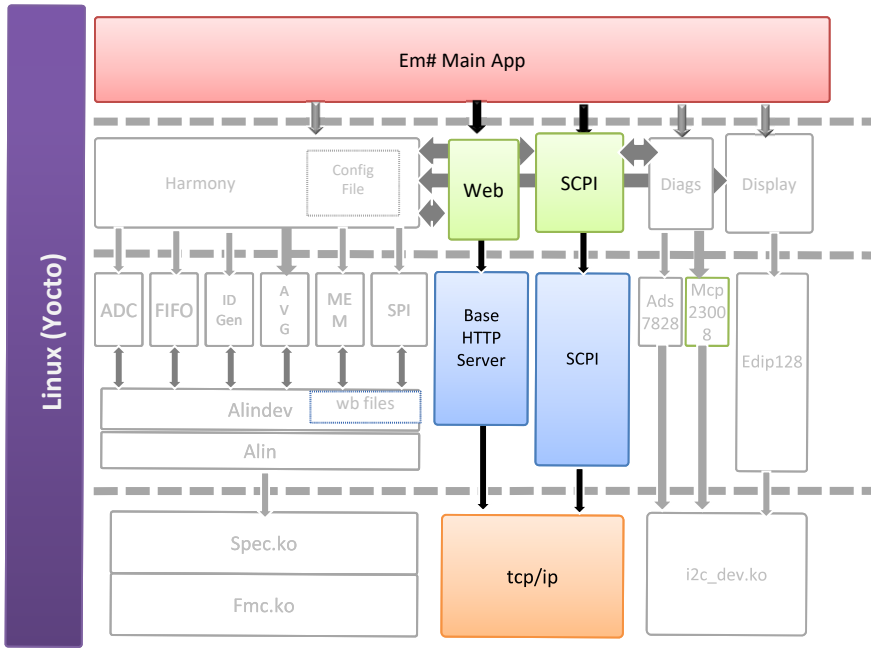


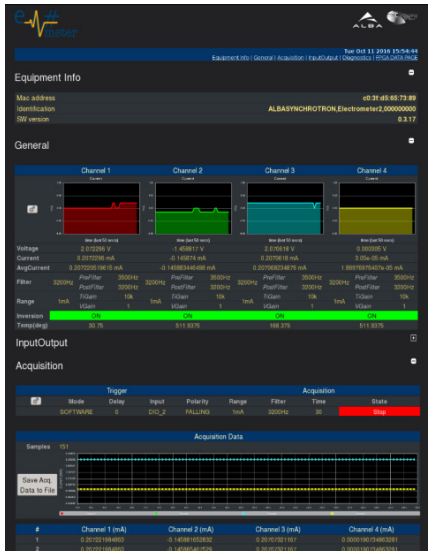
- Main equipment control
  - In the middleware **Harmony Control** module.
    - Configures the acquisition
    - Starts/stop it
    - Process the acquired data in the FPGA memory.
    - Use of an external configuration file with predefined parameters.
  - Specific FPGA block drivers contain commands like init, start, read data,..
  - **Alindev.py** individual control of FPGA blocks
    - Access to configuration parameters
    - Data access through virtual memory address.
    - Device pickle files containing the register map (SDB structure)
  - **Alin.py** gets the SDB structure.
    - Available blocks in the FPGA
    - Virtual memory addresses for each block.
  - **Spec.ko** and **Fmc.ko** linux kernel drivers (source code provided by OHR) provide FPGA access

3. Main control software – ALIN (6/7)

❖ Remote monitoring & control

- ➢ Via Communications ports 5025:
  - ○ ASCII commands that follow the Standard Protocol for Programmable Instruments (**SCPI**).
  - ○ List of commands and their corresponding call-back in **SCPI middleware** while protocol in **SCPI driver.**
- ➢ SSH:
  - ○ Expert control for designers
  - ○ Handful set of tools to check/configure the FGPA

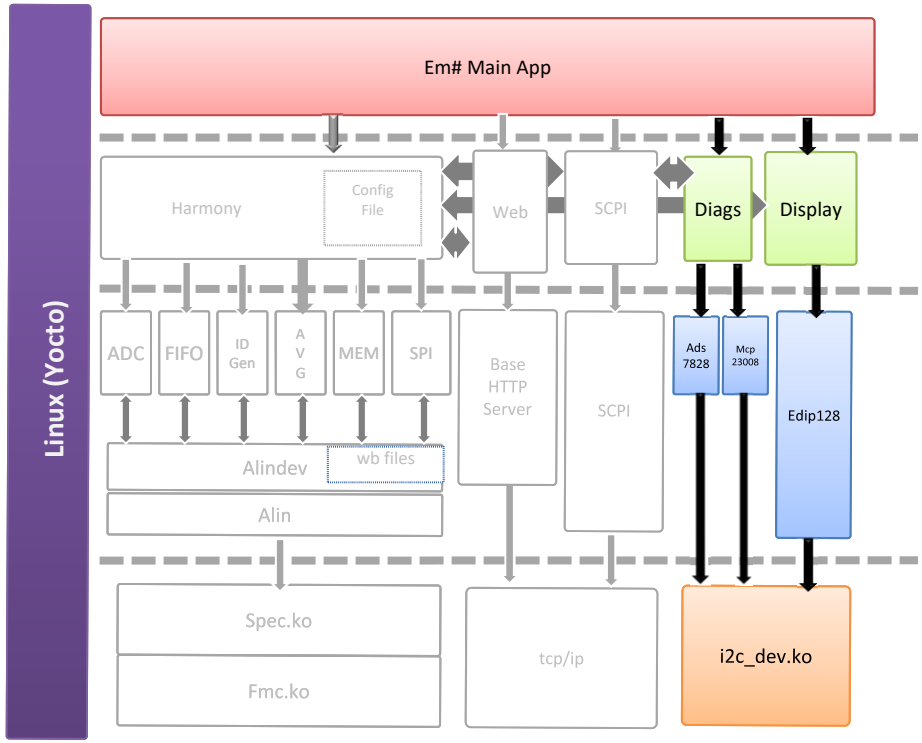




- ➢ Via Web (port 8888)
  - ○ **Webserver middleware** starts/stops the server and generates data JSON file periodically.
  - ○ Web contents updated in browser client using JavaScript and jQuery to read the JSON file.
  - ○ POST PHP method is used to execute equipment commands in server side.

3. Main control software – ALIN (7/7)

- Diagnostics
  - Check the harmony bus stability
  - Check FPGA cores failures
  - PSB board control and consumption self-detection using **Ads7828** (ADC) and **Mcp23008** (Port-Expander) drivers via I2C.
- Local control
  - Through the touch-screen display.
  - Navigation menus allowing user control in the **Display middleware.**
  - High-level language communication protocol via I2C in the **edip128 driver**.



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- Em# achieves unique characteristics in an electrometer (accuracy, bias voltage, processing capabilities…) with a reduced cost
- The software project is modular and easy to adapt to any other similar hardware approach.
- Easy integration into any control system.
- Clear separation between FPGA and SBC responsibilities
  - Configuration and control resides in the SBC
  - Data acquisition in the FPGA.
- Functionality not limited to work only as an electrometer
  - It can be easily adapted and extended

Questions / Comments?

Manuel Broseta
Computing Division
mbroseta@cells.es
+34 93 592 4464

See you soon….