

Controls Architecture for the Diagnostic devices at the European XFEL

Olaf Hensler DESY – MCS Hamburg, Germany







Outline

- European XFEL
- µTCA Hardware
- IPMI monitoring and control
- DOOCS server organisation
- Messaging and data handling
- Status/Schedule
- Conclusion









- Scalable modern architecture
 - From 5 slot single ... 12 slot double size
- High availability
 - Redundant power and fan optional
 - Well defined management
- Differential links only: high analog signal processing quality



 $A = \frac{E[\text{Uptime}]}{E[\text{Uptime}] + E[\text{Downtime}]}$





- XFEL will be based on the new MicroTCA.4 standard
 - Double size Advanced Mezzanine Card (AMC) modules with complex FPGA and PCIe link to CPU
 - Rear Transition Modules for signal conditioning
 - Precise clock and trigger over the backplane





XFEL XFEL Timing System: 1. Prototype

- New Timing System
 - Fiber optic links 1.3GHz
 - with drift compensation
 - AMC prototype is receiver and transmitter
 - ps stability (< 5ps RMS)
 - Clock, trigger and event distribution
 - Double height version under test

1.3GHz































The Intelligent Transport Layer

- The socket library that acts as a concurrency framework
- Faster than TCP, for clustered products and supercomputing
- Carries messages across inter process communication(IPC), TCP, and multicast
- Connect N-to-N via fanout, pubsub, pipeline, request-reply
- Asynchronous I/O for scalable multicore message-passing apps
- Large and active open source community
- 30+ languages including C, C++, Java, .NET, Python

It was easy to integrate into our DOOCS system It runs stable

Fast and reliable reconnects after restarts of processes in the chain



European XFEL Controls Architecture for the Diagnostic devices at the European XFEL SIS300 DMA server @ FLASH



Raw Signal from ADC 90000 samples == 830µs

Raw Signal from ADC Zoomed in to show 3 bunches







Charge reading from Toroid server 220 Bunches 1MHz RepRate

Charge reading from Toroid server Zoomed in around first bunches





- On Core-Duo 1.5 GHz CPU (low end CPU)
- Source Code not yet optimized
 - Additional buffer copy into Messaging system
- **Test results** (90KB buffer, 108 MHz sampling, 10Hz operation)
 - SIS8300 DMA server with 10 ADC channels
 - → ~6 % CPU usage
 - Toroid Server with 10 locations
 - → ~12 % CPU usage
- Latency from Driver to toroid-server (all processing included)
 - ~4ms for one channel
 - ~22ms for 10 channels
- => only little overhead by the Messaging system





- Hardware available
- Messaging Software based on ØMQ is include in DOOCS server library
 - First successful tests
 - Available since May 2012
 - XFEL Timing system
 - First hardware is available
 - DOOCS Server available since May 2012
 - Connection to FLASH timing is done since June 2012
 - DMA Server for SIS8300 including Messaging Software under development
 - First test are done
 - Toroid Server including Messaging Software under development
 - First successful test are done





- XFEL fast diagnostics and controls will be based on µTCA[™]
- ØMQ message passing is included in the DOOCS core
- Hardware and Software tested and proven
- Complete installation planned for spring 2013 at FLASH
- FLASH2 will run with *µTCA*[™] after the shutdown in summer 2013
- XFEL installation in 2013/2014



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XFEL Thank You for Your Attention!

More Info: http://doocs.desy.de





Nov. 2012

Oct. 2009

DESY - MCS, Hamburg, Germany **Olaf Hensler** PCaPAC 2012, 4 - 8 Dec. 2012, Kolkata, India

