

# Digital Pulse Processing Techniques for High Resolution Amplitude Measurement of Radiation Detector

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# Outline



- 1** Introduction.....●
- 2** Design and Simulation.....●
- 3** Implementation.....●
- 4** Experimental Results and Analysis.....●
- 5** Conclusion & Future scope.....●



# Introduction



## Objectives

- ❖ To extract the energy information of the radiation deposited on a detector, in nuclear physics experiment using digital pulse processing techniques.
- ❖ To digitally design and optimize typical pulse processing features:
  - pulse shaping
  - pole-zero compensation
  - baseline restoration
  - pile –up rejection
  - peak detection
- ❖ To implement the designed digital pulse processing system on hardware.



# Introduction



## Motivation

- ❖ In the past few years, traditional analog pulse processing system for nuclear spectroscopy is continuously being replaced by digital systems because of:
  - Better performance
  - Stability
  - Feasibility
  - Low cost.
- ❖ It is required to develop such a digital pulse processing system for the various nuclear physics experiments carried out in VECC, whose performance can reach up to satisfactory level to replace it with traditional analog systems already being used.



# Introduction



## Proposed Approach

- ❖ In digital pulse processing technique, preamplifier output signals are directly digitized and processed to extract energy information of particle.
- ❖ Costly peak sensing ADC is replaced by low cost fast ADCs.
- ❖ Traditional analog electronics is here replaced by programmable digital filters.
- ❖ Most of the typical processing features are optimally designed and implemented using programming codes.
- ❖ Two digital pulse processing techniques are proposed and demonstrated -
  - ***Software based digital pulse processing using 'C' programming***
  - ***Hardware based digital pulse processing using VHDL.***

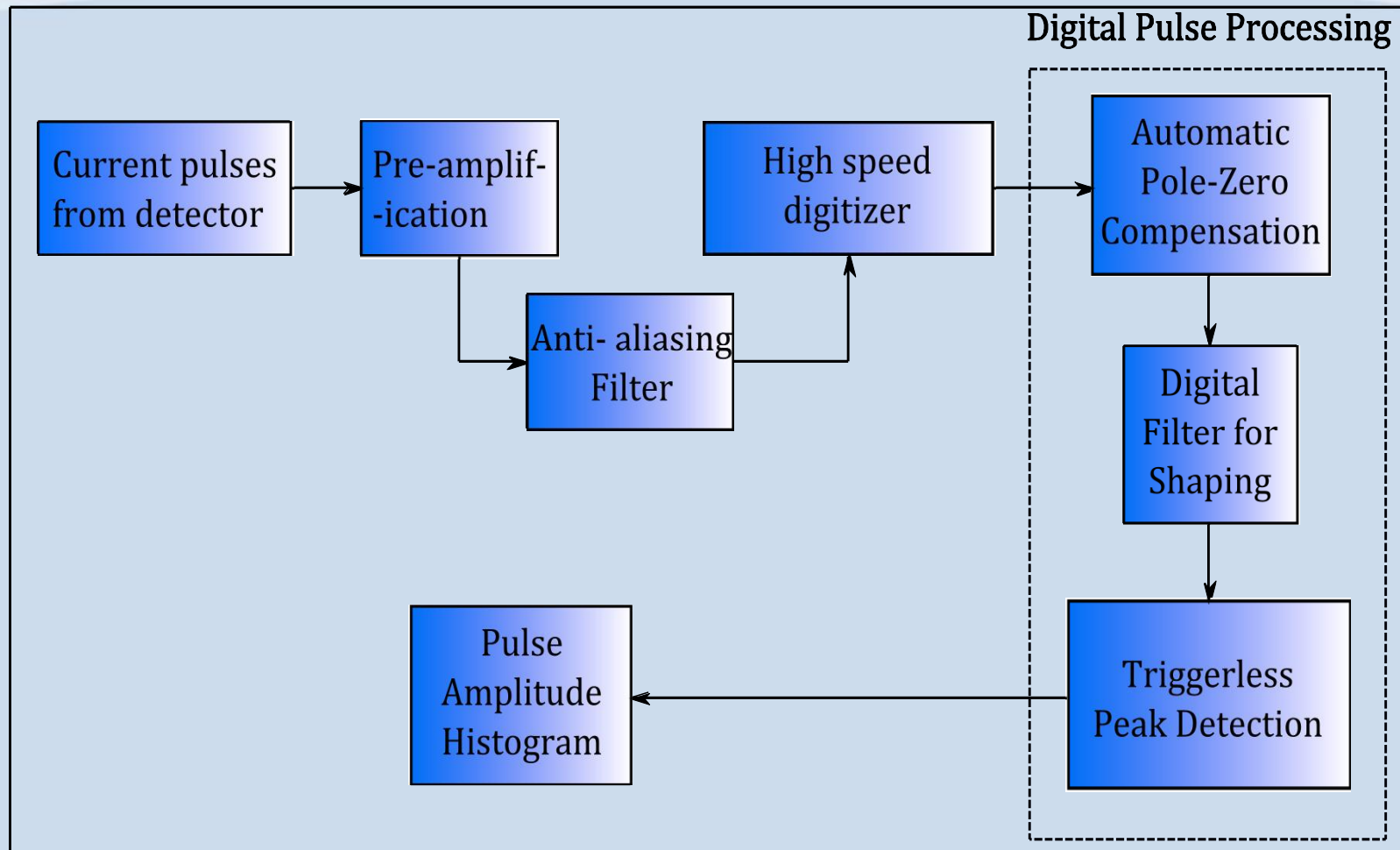




# Introduction



## Proposed Approach



# Design and Simulation

## Digital filter for CR-RC shaping and P-Z compensation

### ❖ Steps of design:

- Specifying ideal filter response in s-domain using prototype analog filter:
  - Define shaping time ( $\tau$ ) of CR-RC filter.
  - Define fall time ( $\tau_f$ ) of preamplifier pulse.
- s-domain to z-domain transformation to generate a set of digital filter coefficients:
  - Select transformation method.
  - Select sampling period  $T_s$ .
- Quantization of floating point coefficients to yield a fixed point response.



# Design and Simulation



## Digital filter for CR-RC shaping and P-Z compensation

### ❖ CR-RC Shaper:

- To attenuate both low and high frequency noises and make the pulse shape convenient for analysis, both CR and RC filters must be employed.
- Of the various pairs of values of time constant, it has been seen that  $\tau_{CR} = \tau_{RC}$  gives best combination of flat pulse top and quick return baseline.
- This condition is also corresponds to maximum signal to noise ratio.
- Transfer function of CR-RC filter is:

$$G_{CR-RC}(s) = TS / (TS + 1)^2$$





# Design and Simulation



## Digital filter for CR-RC shaping and P-Z compensation

### ❖ Pole-zero compensator:

- To eliminate additional pole-zero effect of preamplifier, a compensator should be used whose transfer function is inverse of pre-amplifier transfer functions.
- Transfer function of compensator is:

$$G_{comp}(s) = (T_i s + 1) / T_i s$$

### ❖ Analog Prototype of Digital Filter:

- Combining both CR-RC shaper and compensator, analog prototype of digital filter is represented by:

$$G_{filter}(s) = T (T_i s + 1) / T_i (T s + 1)^2$$



# Design and Simulation



## Digital filter for CR-RC shaping and P-Z compensation

### ❖ Transformation from s-domain to z-domain:

- Mapping from the continuous s-domain to the z-domain should be accomplished by a consistent transformation with the best possible linear correspondence between analog and digital angular frequencies.
- This feature is a characteristic of the bilinear transformation:

$$s = 2(z-1)/T_s(z+1)$$

### ❖ Selection of sampling time $T_s$ :

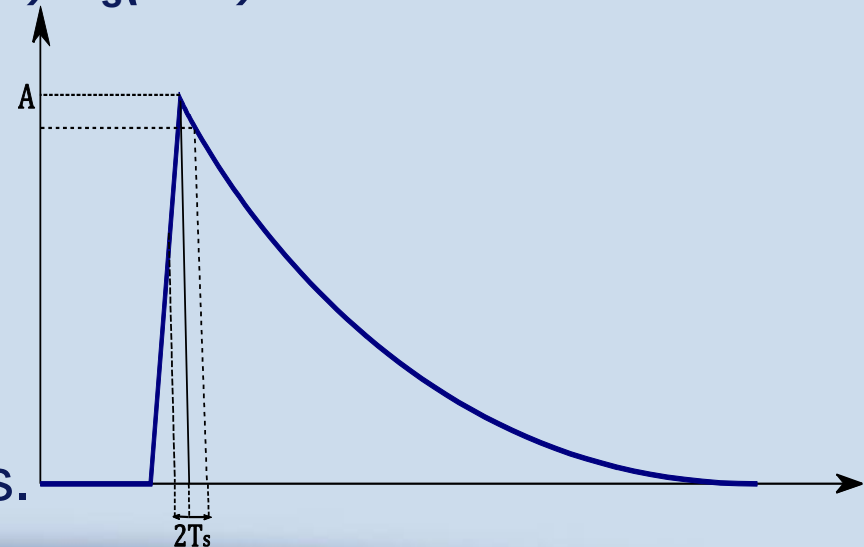
- Maximum possible error:

$$A - A \exp(-T_s/\tau)$$

- For 0.1% of error:

$$T_s = 0.001 \tau$$

- $T_s$  should be order of 10 -20 ns.



# Design and Simulation

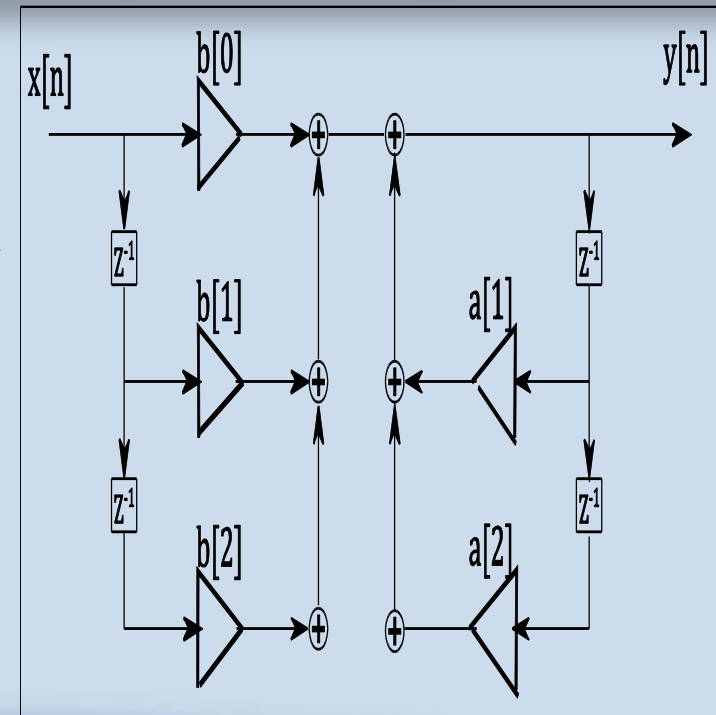
## Digital filter for CR-RC shaping and P-Z compensation

### ❖ Realization of digital filter

- Difference equation of digital filter is:

$$y(n) = a_1 y(n-1) + a_2 y(n-2) + b_0 x(n) + b_1 x(n-1) + b_2 x(n-2)$$

- Equation represents a digital IIR filter.
- Shaping time of filter is decided by coefficients  $a_1$  and  $a_2$ .
- Pole-zero compensation depends on  $b_0$ ,  $b_1$  and  $b_2$  for a certain sampling period.

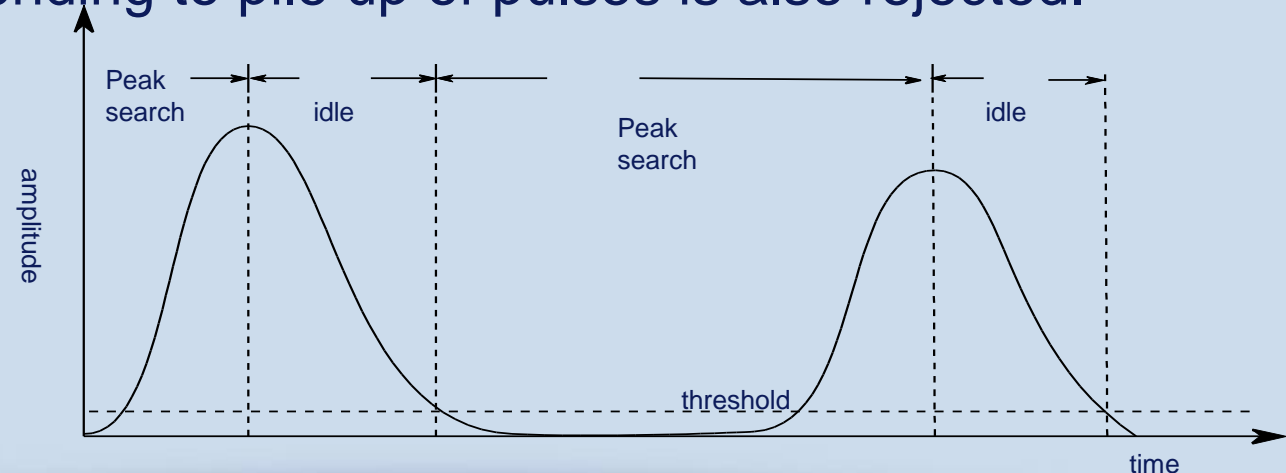


# Design and Simulation



## Peak Detection

- ❖ Peak is detected at the rising edge of filter output pulse by comparing each sample.
- ❖ The largest sample is considered as peak and once peak is detected no action is performed at falling edge until sample goes below a threshold indicating end of pulse.
- ❖ Rejection of false peak because of presence of noise is also taken care.
- ❖ Peak corresponding to pile up of pulses is also rejected.

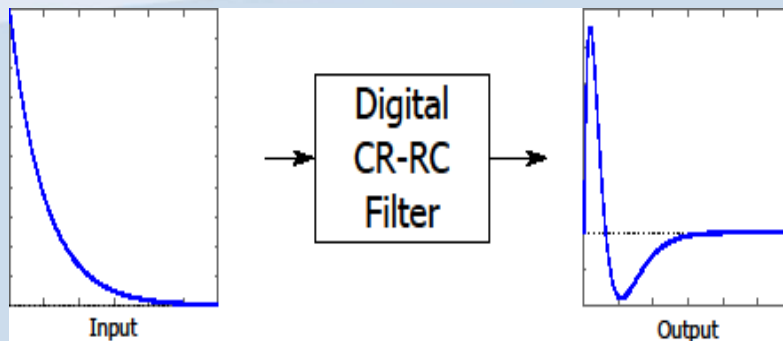


# Design and Simulation

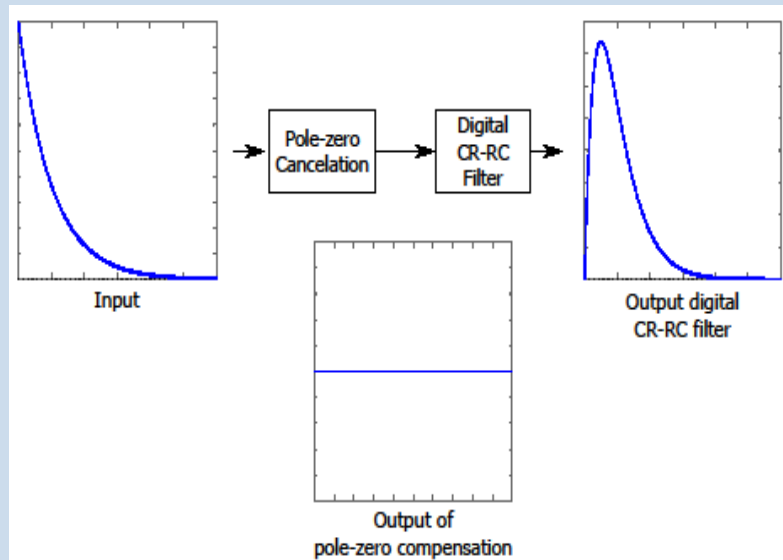
## Simulation Results



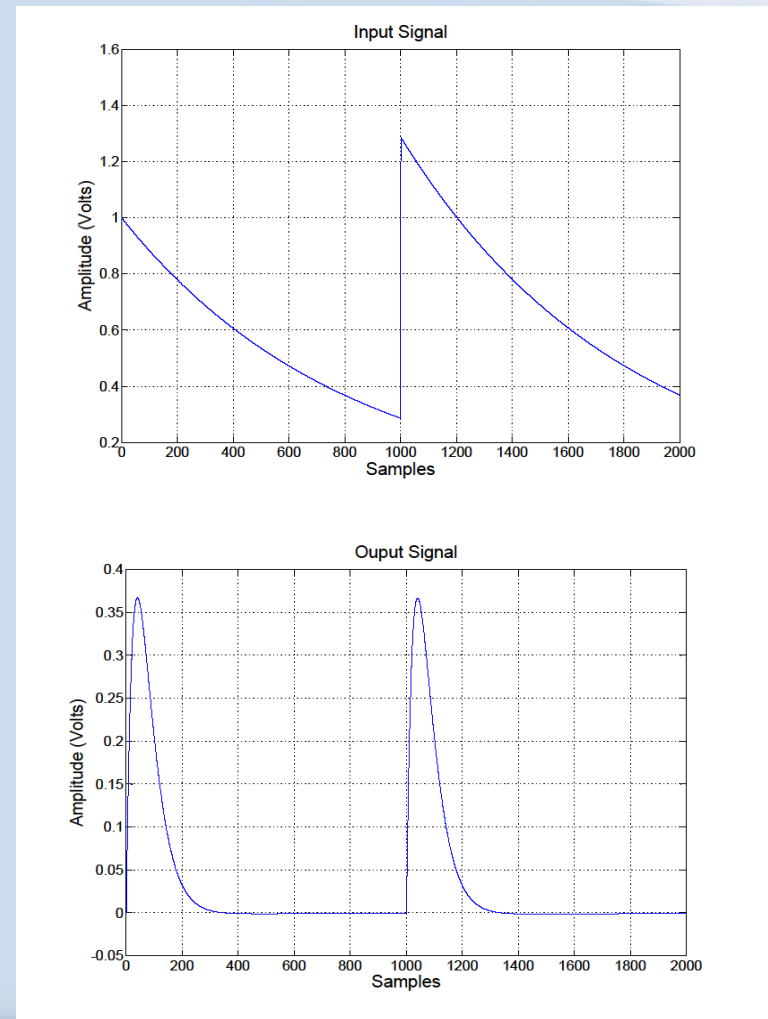
### ■ Without Compensation



### ■ With Compensation



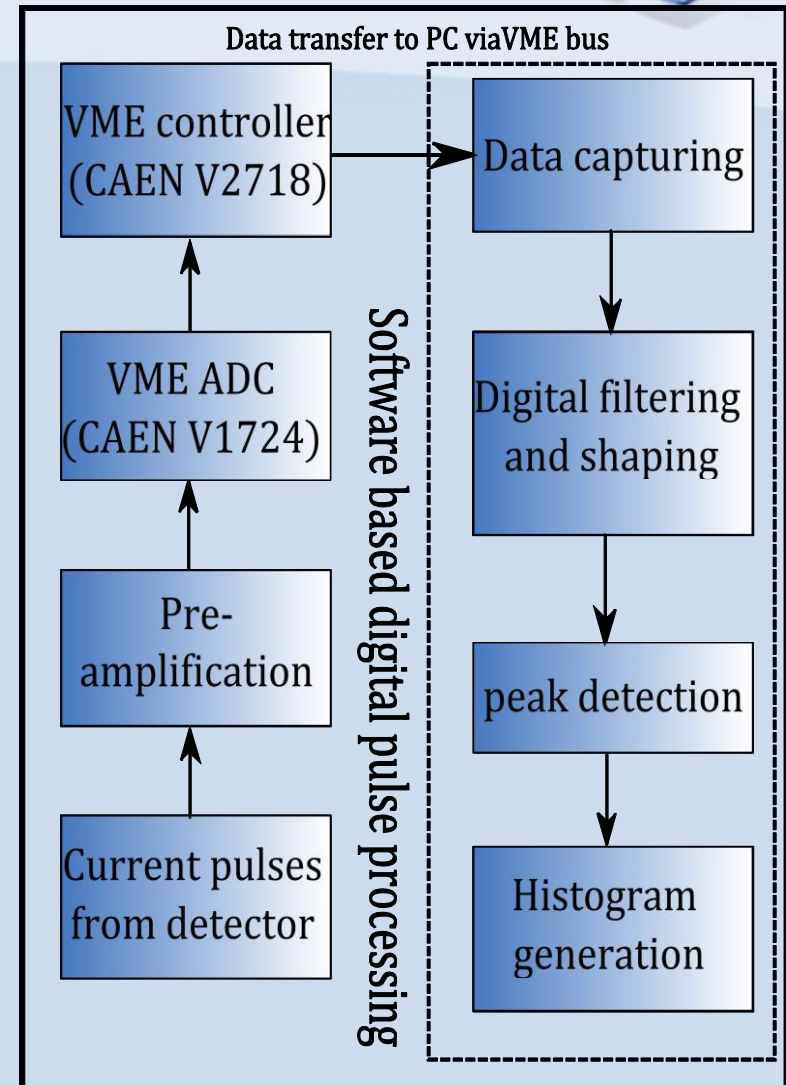
### Input and output of digital filter



# Implementation

## Software Based System

- ❖ Data is sampled by a 14 bit 100 MSPS VME ADC. The data stream is continuously written in a circular memory buffer and read via VME.
- ❖ Data is acquired through block transfer mode at the cost of loss of many events.
- ❖ Fragmented data is discarded at the beginning and end of the block.





# Implementation



## Software Based System

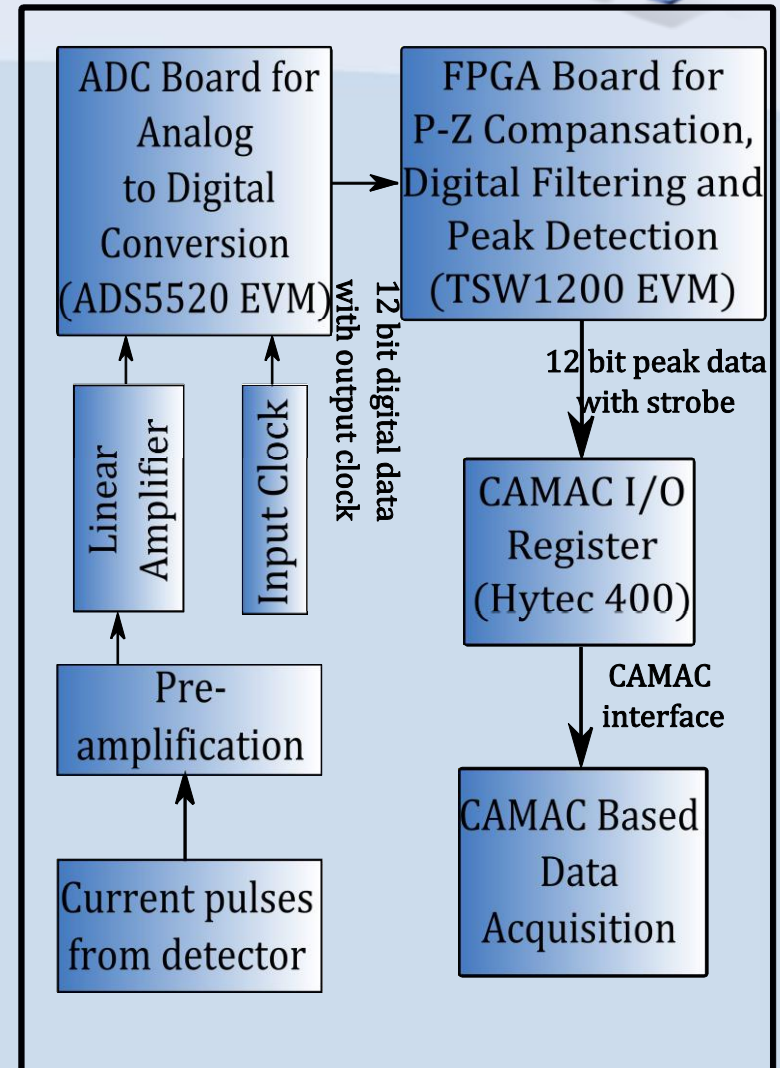
- ❖ All pulse processing features are designed at software level using 'C' programming.
- ❖ Various pulse processing features can be easily modified and tested by varying the parameters for various detector systems and various ADCs.
- ❖ 'C' codes are written to implement digital filters for CR-RC shaping of pulse, along with pole-zero compensation.
- ❖ A trigger less peak detection logic is developed to measure amplitude of filtered pulse.
- ❖ False peak due to noise and pile-up are eliminated.
- ❖ Peak is plotted on histogram to analyze energy information of particle.



# Implementation

## Hardware Based System

- ❖ Pulse processing blocks used in software based system is translated into a hardware system for real time implementation.
- ❖ A continuous running, trigger-less, digital system is optimally designed and implemented at hardware level to perform typical processing tasks.
- ❖ This system is having advantage of zero dead time and no loss of events.



# Implementation



## Hardware Based System

- ❖ Spectroscopy performances are achieved using low-cost and relatively low-resolution (12-bit) AD converters at high sampling frequency (80-100MSPS).
- ❖ For current implementation, XC4VLX25 Virtex 4 FPGA has been chosen, which would be feasible to implement the system to withstand ADC throughput rate.
- ❖ VHDL codes have been written for automatic detection of fall time, digital IIR filter for pulse shaping and peak detection.
- ❖ All these codes are synthesized and implemented on FPGA using Xilinx ISE 10.1 EDA tool.
- ❖ Output of peak detection is read by CAMAC based data acquisition system and plotted on histogram for further energy analysis.

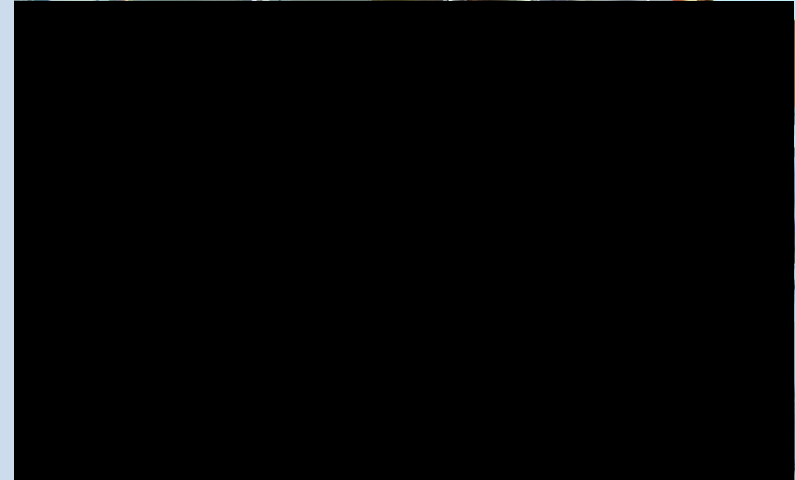


# Experimental Results



## Experimental Setup

- ❖ To validate the performance of proposed systems, we have used various input from pulse generator and semiconductor detectors with radioactive sources.
- ❖ In order to measure the resolution of proposed digital systems, HPGe detector (resolution 2 KeV) is used, with  $^{60}\text{Co}$  source.
- ❖ It emits two groups of gamma rays having energy 1173KeV and 1332KeV .



# Experimental Results



## Experimental Setup

- ❖ A linear amplifier with no pulse processing feature is used with both the digital systems to enhance the preamplifier output signal.
- ❖ Digital filter was designed with shaping time  $6\mu\text{s}$  and automatic pole - zero compensation is done for amplified pulse with fall time nearly equal to  $50\mu\text{s}$ .
- ❖ Performances of both the systems are compared with traditional analog gamma spectroscopy system, using spectroscopy amplifier and CAMAC based 13 bit peak sensing ADC (Ortec 413).



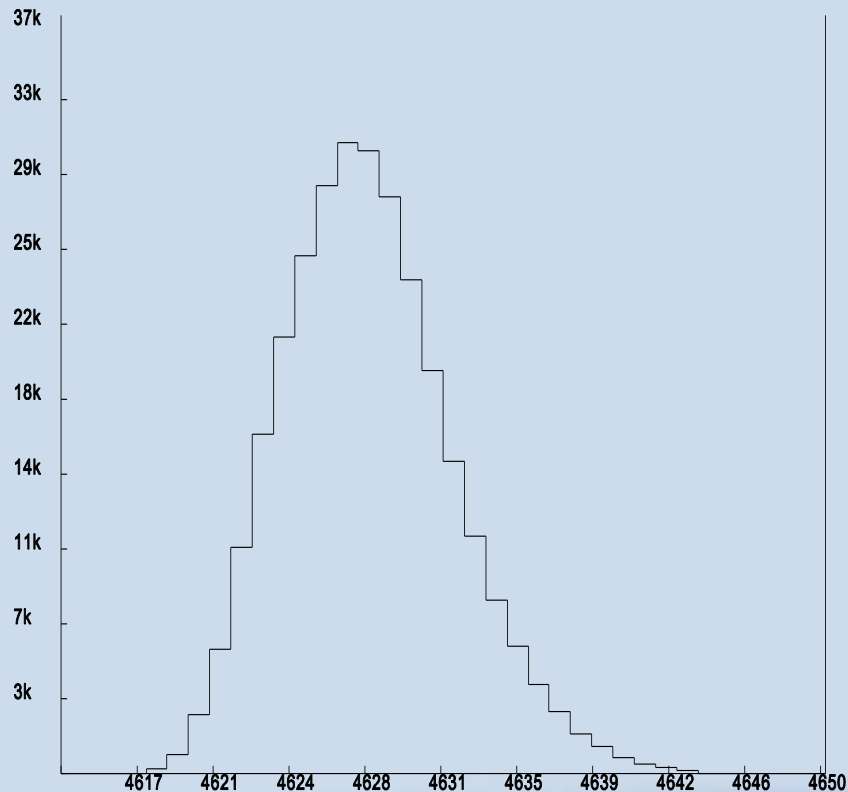
# Experimental Results

## Spectrum obtained from pulse generator



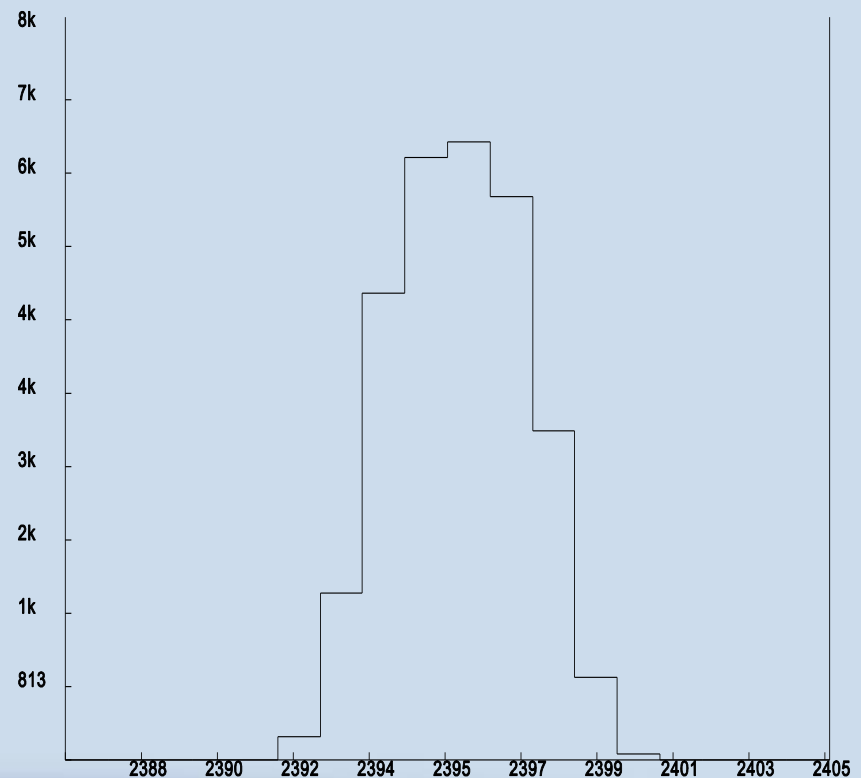
### ■ Without digital filter

- ❖ FWHM is nearly 10 channels
- ❖ Resolution = 0.22%



### ■ With digital filter

- ❖ FWHM is nearly 3 channels
- ❖ Resolution = 0.146%

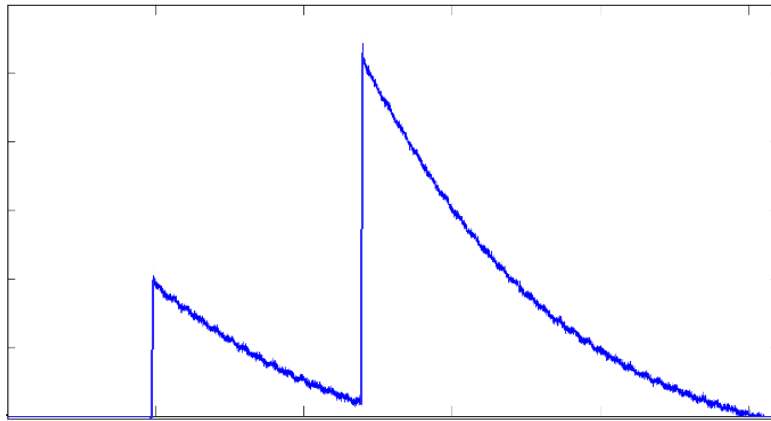




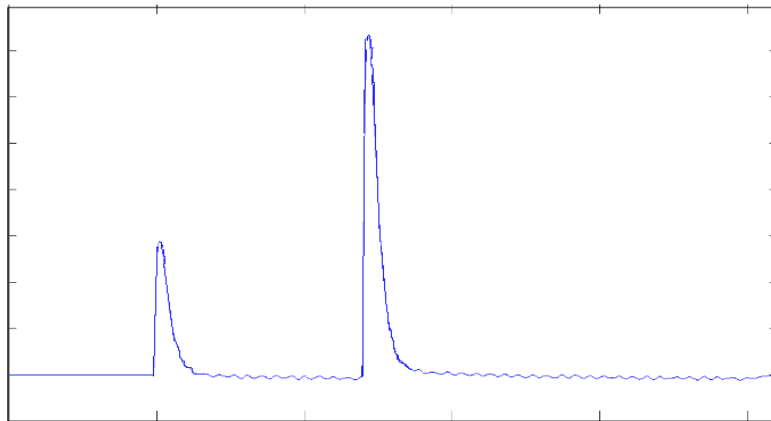
# Experimental Results



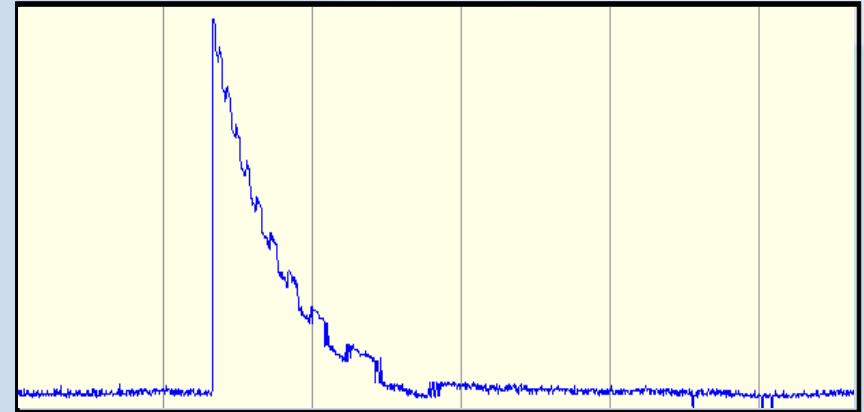
## Output of Digital Filter



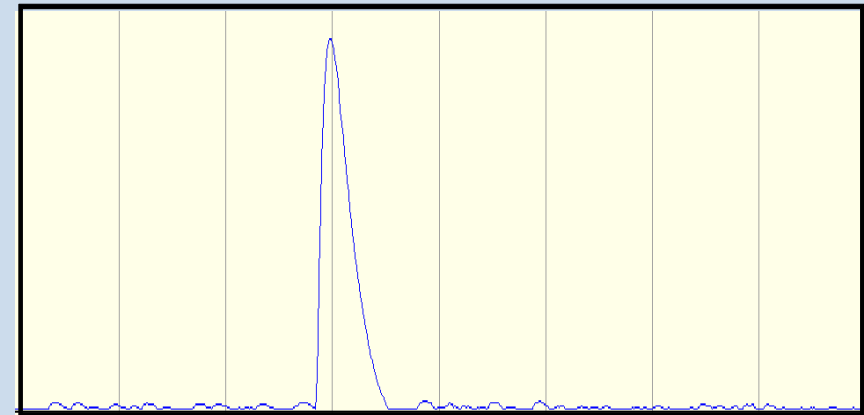
(a)



(b)



(a)

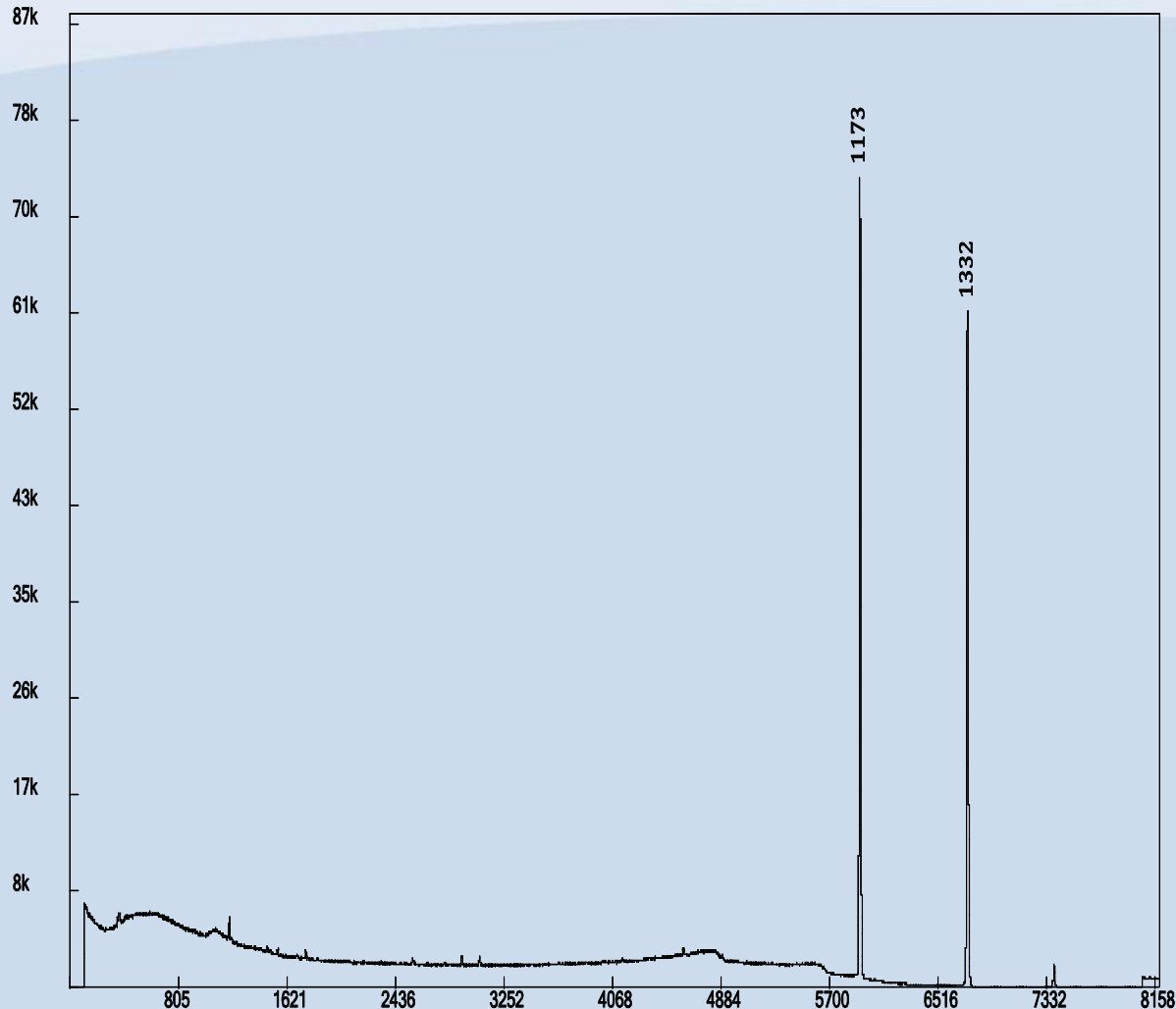


(b)



# Experimental Results

## Spectrum of $^{60}\text{Co}$ using traditional analog pulse processing

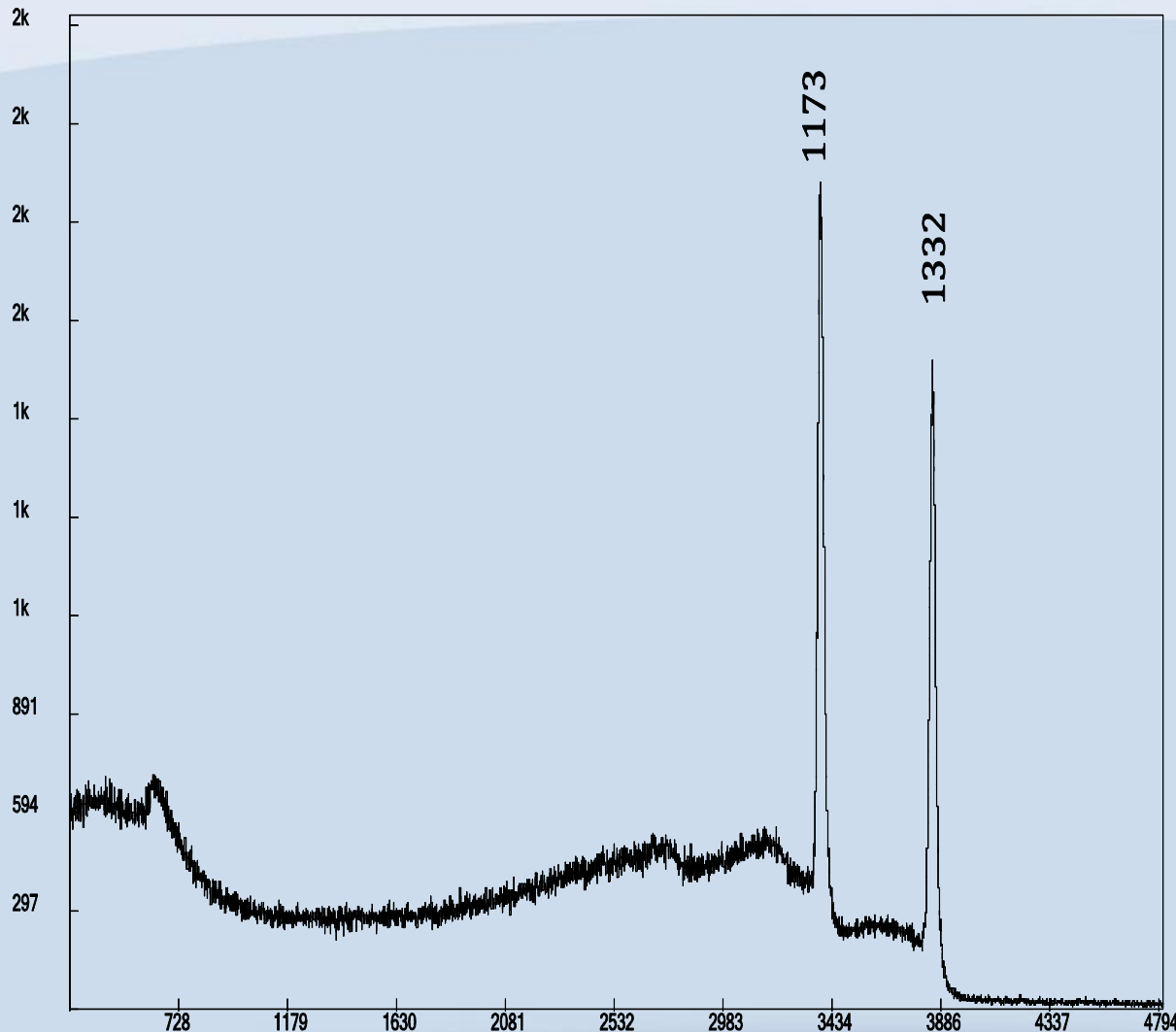


- ❖ Two spectral lines occurs at channel number 5944 and 6752 corresponding to energies 1173 and 1332 KeV.
- ❖ Peak fitting curve at spectral line 1332 KeV, gives an FWHM of 13 channels.
- ❖ Resolution of this system at spectral line 1332 KeV is **0.192%**.



# Experimental Results

## Spectrum of $^{60}\text{Co}$ using VME ADC based pulse processing

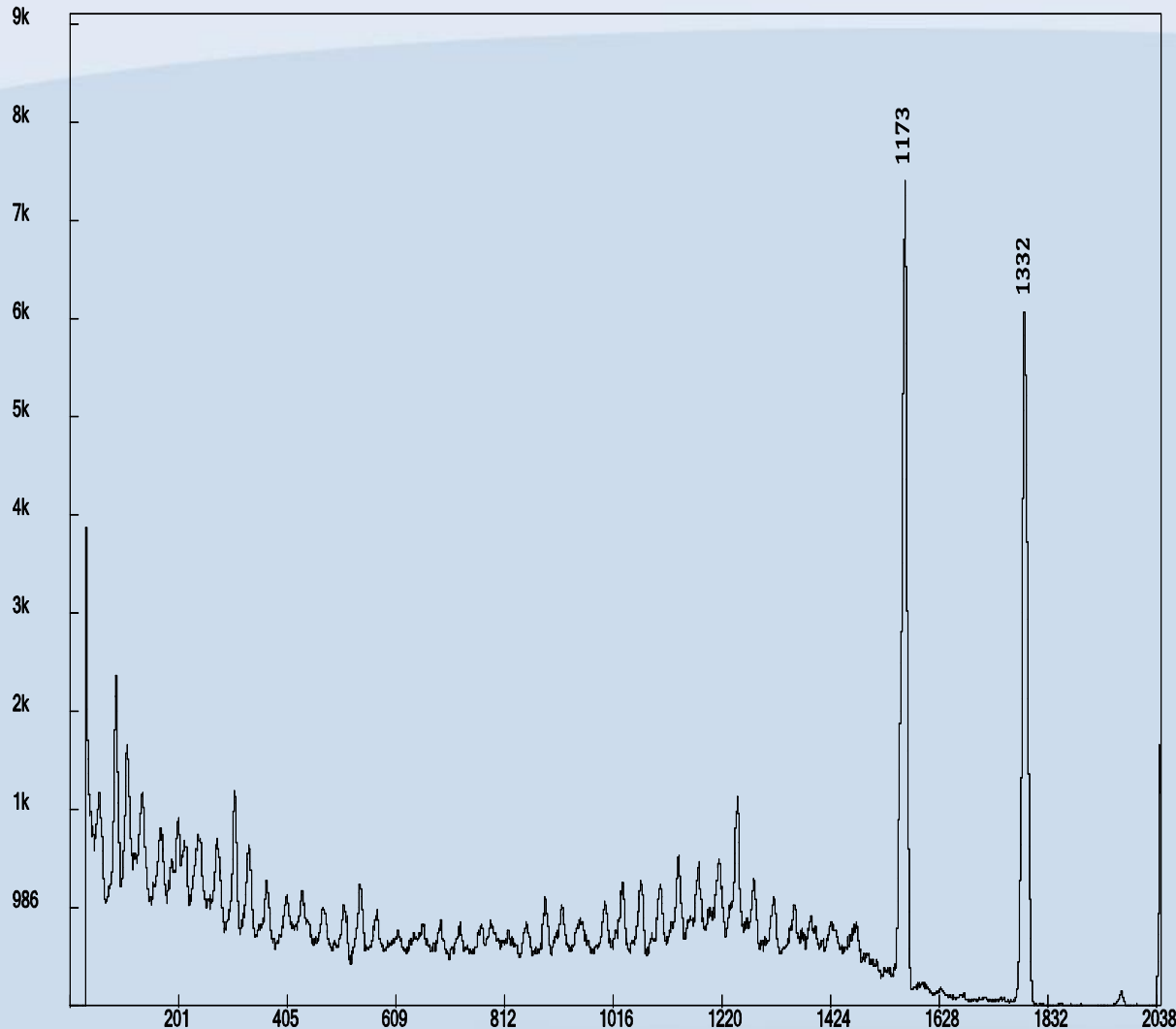


- ❖ Two spectral lines occurs at channel number 3397 and 3859 corresponding to energies 1173 and 1332 KeV.
- ❖ Peak fitting curve at spectral line 1332 KeV, gives an FWHM of 21 channels.
- ❖ Resolution of this system at spectral line 1332 KeV is **0.532%**.



# Experimental Results

## Spectrum of $^{60}\text{Co}$ using FPGA based pulse processing



- ❖ Two spectral lines occurs at channel number 1566 and 1791 corresponding to energies 1173 and 1332 KeV.
- ❖ Peak fitting curve at spectral line 1332 KeV, gives an FWHM of 11 channels.
- ❖ Resolution of this system at spectral line 1332 KeV is **0.578%**.



# Conclusion and Future Scope



- ❖ The developed digital systems were experimentally tested with various inputs from pulse generator and particle sources using semiconductor detectors.
- ❖ Overall resolution obtained, particularly with FPGA based system, is 0.578%, which shows that the proposed digital system can be used for variety of detectors eg. HPGe, Si detector, NaI detector etc.
- ❖ Obtained resolution appears to be high due to amplitude distortion of digitized input pulse because of malfunctioning of 4<sup>th</sup> bit of ADC and additional noise contributed by external amplifier and ground.



# Conclusion and Future Scope



- ❖ FWHM can be improved by:
  - Using a better fault free ADC.
  - Using an anti aliasing filter at ADC input, to eliminate the contribution of high frequency noise in FWHM.
  - Using CR-RC<sup>n</sup> filter for better SNR, at the cost of low count rate capability.
  - Using a single board for the whole system with proper design and shielding to reduce the contribution of external noise sources.
- ❖ The work can be extended to design a single board including fast digitizer and digital filters implemented on FPGA, for multi-channel system.





**Any Queries ?**

**Thank You !**