DESIGN OF THE DATA ACQUISITION SYSTEM FOR THE NUCLEAR PHYSICS EXPERIMENTS AT VECC

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Outline

- Detector system
- DAQ Requirement
- CAMAC DAQ
- VME DAQ
- Multicrate VME
- Synchronization
- Future Plan
- Conclusion

Large Detector Arrays at VECC

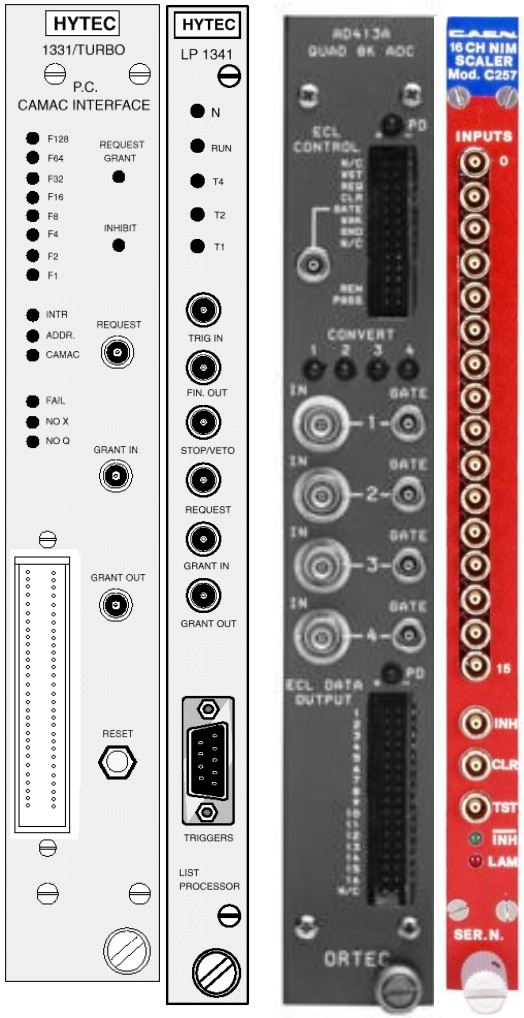
- **Charge Particle Detector Array (CPDA):** 4-π charge particle detectors. It consists of three parts
  - Forward array: 7°-45° with 24 Si-Si-CSI(Tl) telescope
  - Extreme forward array: 3°-7° with 32 Phoswich detectors
  - Backward array: 45°-175° with 330 CSI(Tl) detectors
- **Gamma spectroscopy**
  - Large Area Modular BaF_2 Detector Array (LAMBDA): Study high energy γ-rays with 162 BaF_2 detectors
  - Gamma multiplicity filter array(GAMMA): 50 BaF_2 detectors
- **Neutron detectors:**
  - Neutron Time-of-flight Measurement: 50 detectors
  - Neutron Multiplicity detector

DAQ Requirements

- The DAQ system should able to handle more than 1200 channels.
- Data rate of 1MParameters/sec
- Commercial-off-the-shelf hardware modules
- Support for VME and CAMAC based system on both Linux and Windows machine
- Data storage in zero suppressed mode
- Generation of online 1D and 2D histogram generation & manipulation

CAMAC

- CAMAC: Computer Automated Measurement And Control
- Standardized by ESONE, IEEE/ANSI, IEC around 1972



CAMAC Specification

- 19” Crate, modular hardware form factor, 25 slots to attach modules.
- Crate contains power supply, backplane & FAN unit.
- Slot 25 is for CAMAC Crate controller module. The slot 1-24 may be occupied by CAMAC modules.
- The CAMAC backplane provides +6V, -6V, +24V & -24V, 0V (return) DC power; optionally +12V, -12V, +200V DC and 117V AC power may also be provided
- The Hytec 5331 crate controller with PCI interface card & LP1341 List Processor are used.

CAMAC backplane signals

- CAMAC Data & Address lines:
  - 24bit *READ* & 24bit *WRITE* bus.
  - N – Slot number: each slot is directly addressed by controller with this signal
  - A – sub-address : Each CAMAC module can host 16 sub-unit
  - F – Function: Each sub-unit can perform 32 functions
- Control signals
  - S1, S2: Timing signal for dataway operations
  - Z: Initialize

CAMAC backplane signal

- C: Clear
- B: Busy
- I: Inhibit

- Module responds with signals:
  - L: Look At Me (LAM) signal. L line individually connects each slot to the controller, works as a interrupt to controller.
  - Q: asserts the operation status
  - X: asserts the command has been accepted

CAMAC Cycle

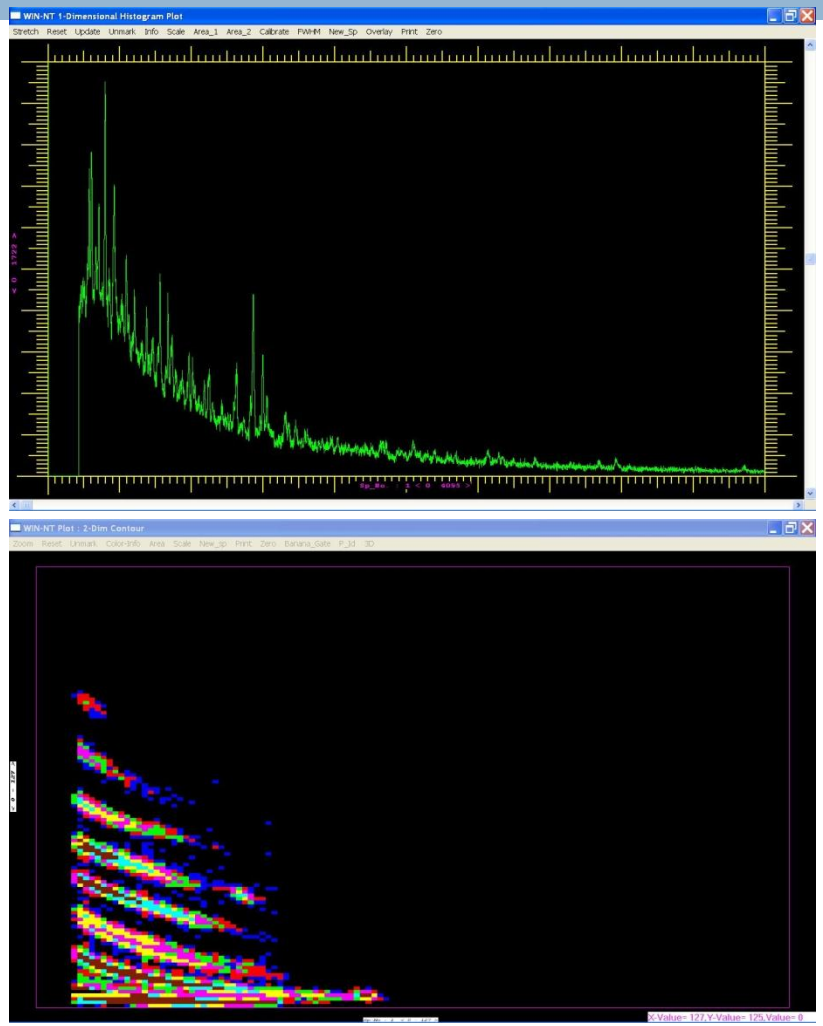
- The typical CAMAC cycle takes minimum 1μsec.
- If a 24bit Data is read in each cycle, maximum theoretical throughput will be 3MB/sec

Hytec CAMAC Controller

- The total read/write time from DAQ software involves interrupt latency, software overhead and the CAMAC cycle time
- Hytec controller on Linux takes on an average 10μsec
- With List processor the average time can be 2.14μsec

CAMAC DAQ Software

- CAMAC DAQ on Linux and Windows
- t4: First PC based Win16 Win3.1using WinSDK
- t32 for Win32 systems Windows 98/2000/NT/XP
- Offline version st32 and ast32, offline



VME

- VME: Versa Module Eurocard
- Maintained by VITA http://www.vita.com

VME64X system

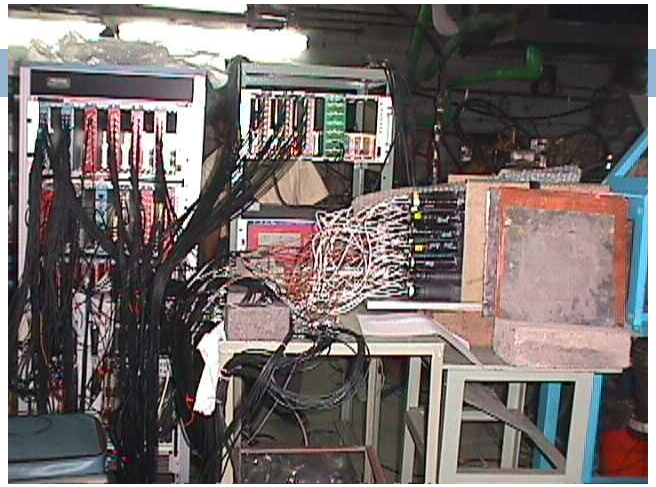
- 19” crate with power supply unit & FAN unit
- Crate’s height and depth depend on form-factor. 3U, 6U and 9U crates (1U=1.75”) are available
- 6U VME64x crate has 21 slots and common backplane for all the signal and power lines
- p1 & p2 160pin and p0 is 95pin connector for each module
- +5V, +12V, -12V, +3.3V DC power are available in VME64X crate
- Hot-swappable, User IO

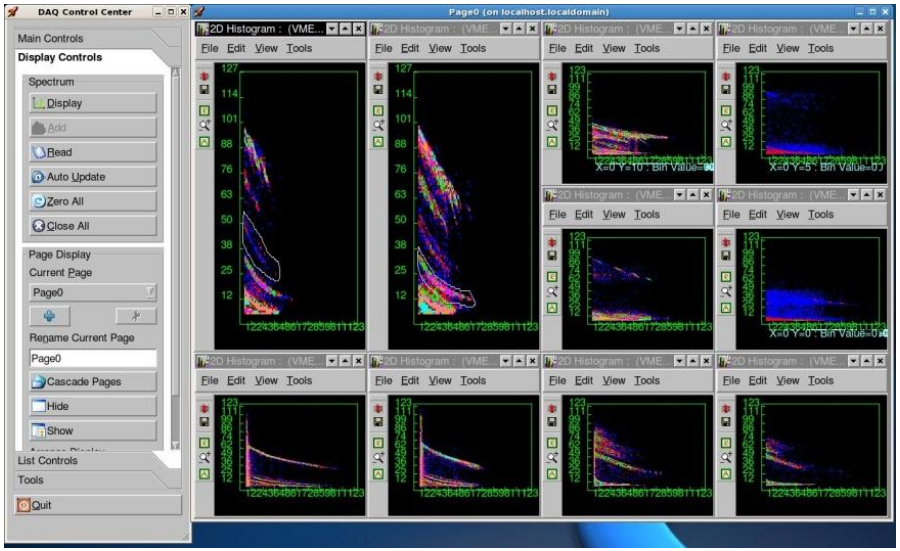
Salient feature of VME Bus

- Asynchronous BUS, Master/slave architecture
- Memory mapped IO
- Supports Multiprocessors, interrupt capability
- Slot 1 is for controller/arbitrator unit
- Data bus 32bit, Address bus 32 bit, Priority Interrupt bus, Arbitration bus, Utility bus
- Multiplexed bus operation makes it possible for 64bit data and 64bit address operation
- 100ns bus cycle. Supports 40MB/sec data rate for 32bit. Multiplexed mode supports 80MB/sec data rate.

VME DAQ System

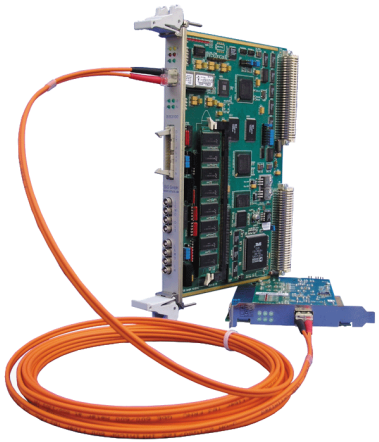
- The VME DAQ is developed in C++ and QT3 toolkit on both Linux and WindowsXP/2003
- SIS3100, CAEN V2718
- Controllers are interface with PCI card and fibre optics cable
- Block trasfer rate 5-7MB/sec for 32bit.



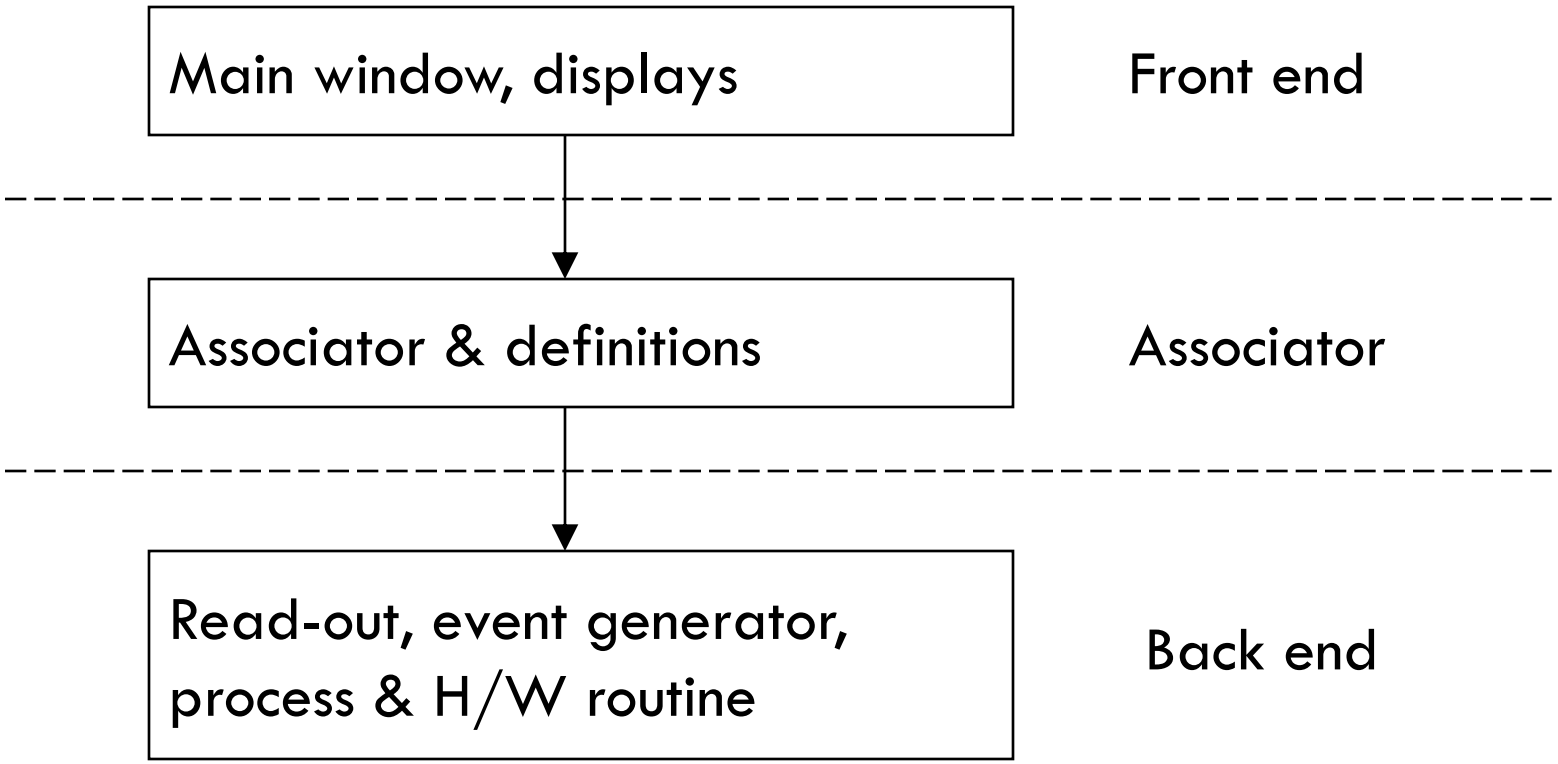


VME modules

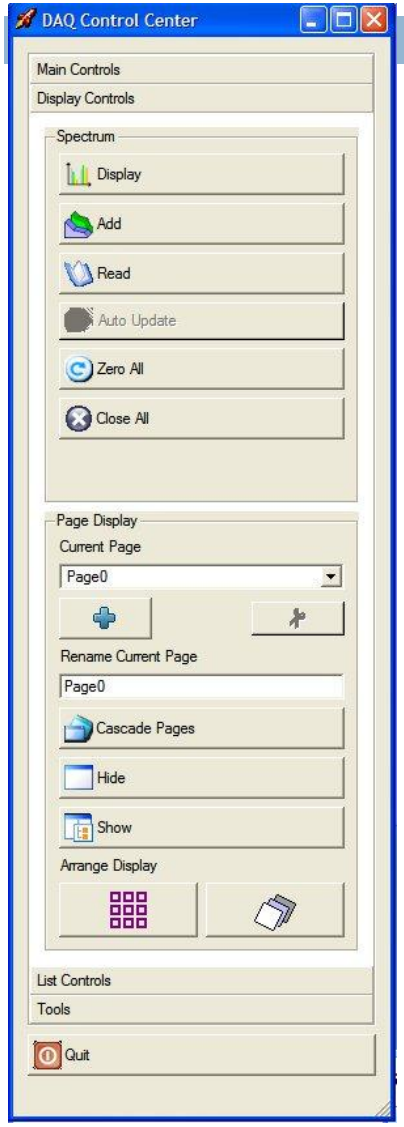
- CAEN VME785, 792 & 775
  - 32 channel 12bit resolution
  - 5.7us ADC conversion time for all 32channels
  - 32event FIFO memory
  - External ECL bus for control and synchronization
  - BLT32, CBLT and MBLT capable
- MDI2, MADC32 from mesytec

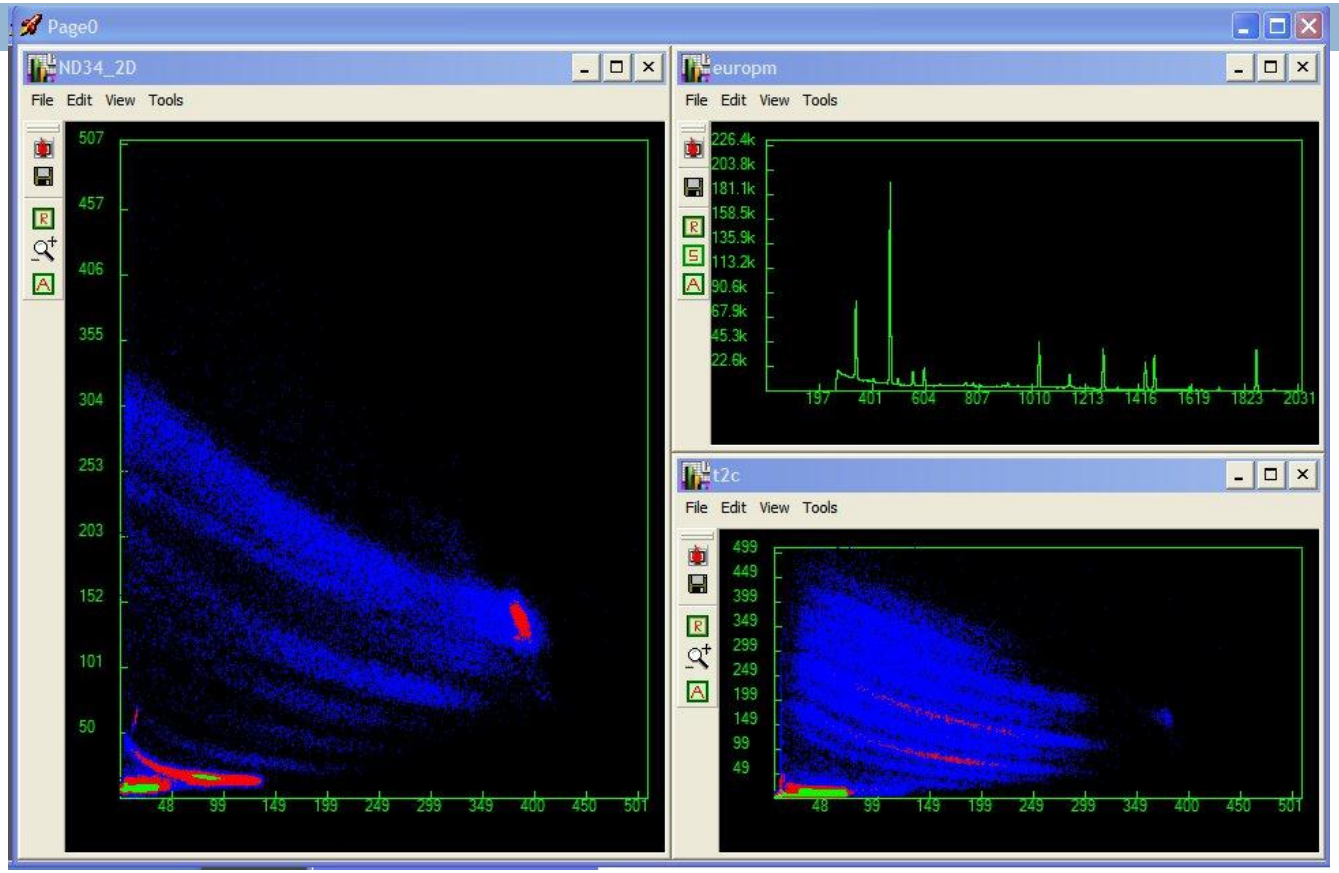


Layered Architecture



VME DAQ Software





Configuration file

- C-style Single configuration file for complete configuration, compatible to both offline and online
- Define module, function, system, conditional construct

```
module{
                module_type=vme785;
                base_address=0x800000;
                instance=0;
               channel=32;
                conversion_gain=4096;
                event_size=34;
                geographical_address=4;
}
```

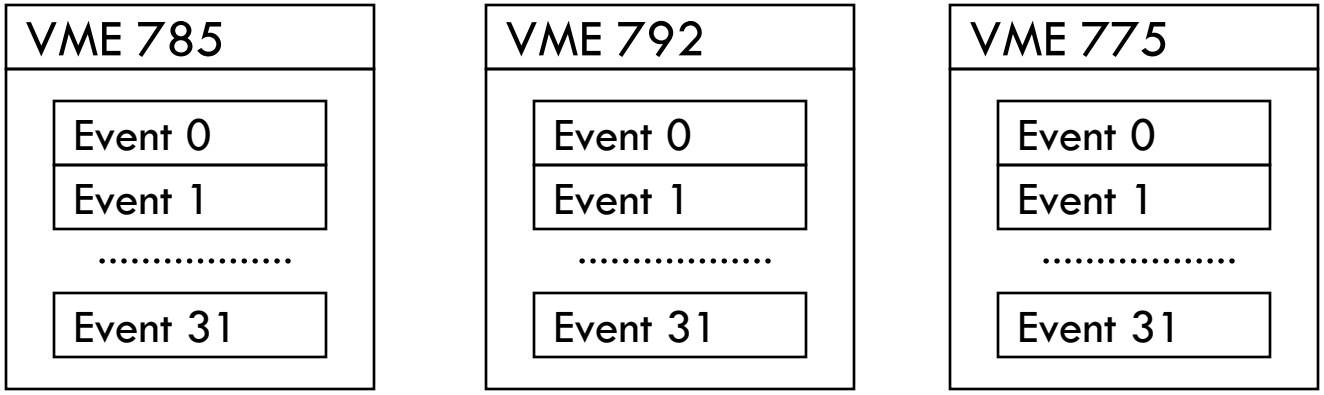
```
system{
 transfer_mode=CBLT;
 no_of_crates = 2;
event_trigger = 30;
}
```

```
function{
 func_type=oned;
 spec_len=4096;
 gain=1.0;
 offset=0.0;
 channel_no0{
    module_type=vme785;

    instance=0;
    channel=0;
  }
}
```

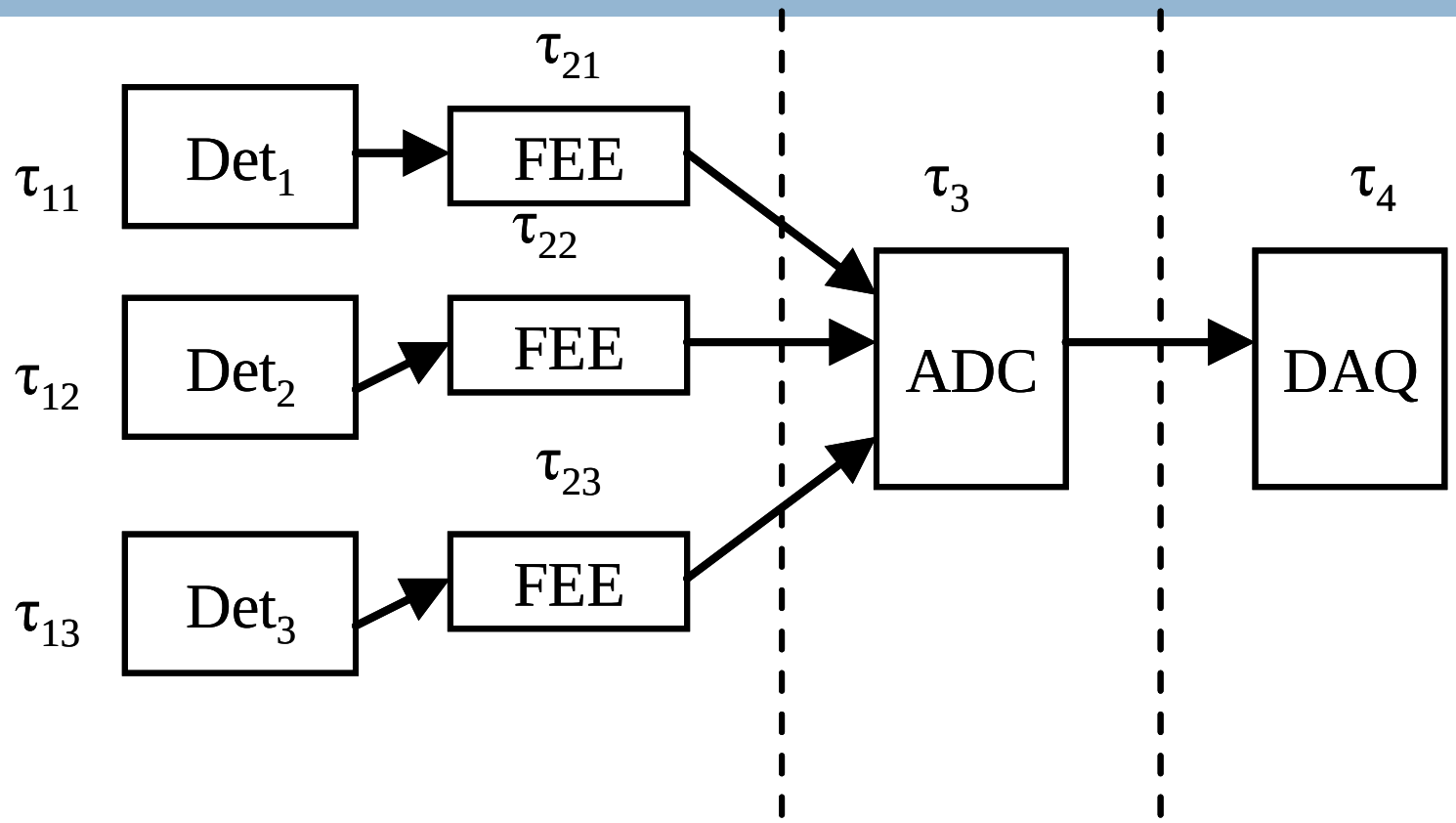
```
if(1 & 2)
{
 function{
    func_type=twod;
    x_len=512;
    y_len=512;
  channel_no0{
                module_type=vme785;
                instance=0;
                channel=16;
   }
  channel_no1{
                module_type=vme785;
                instance=0;
                channel=25;
   }
 }
}
```

Readout scheme



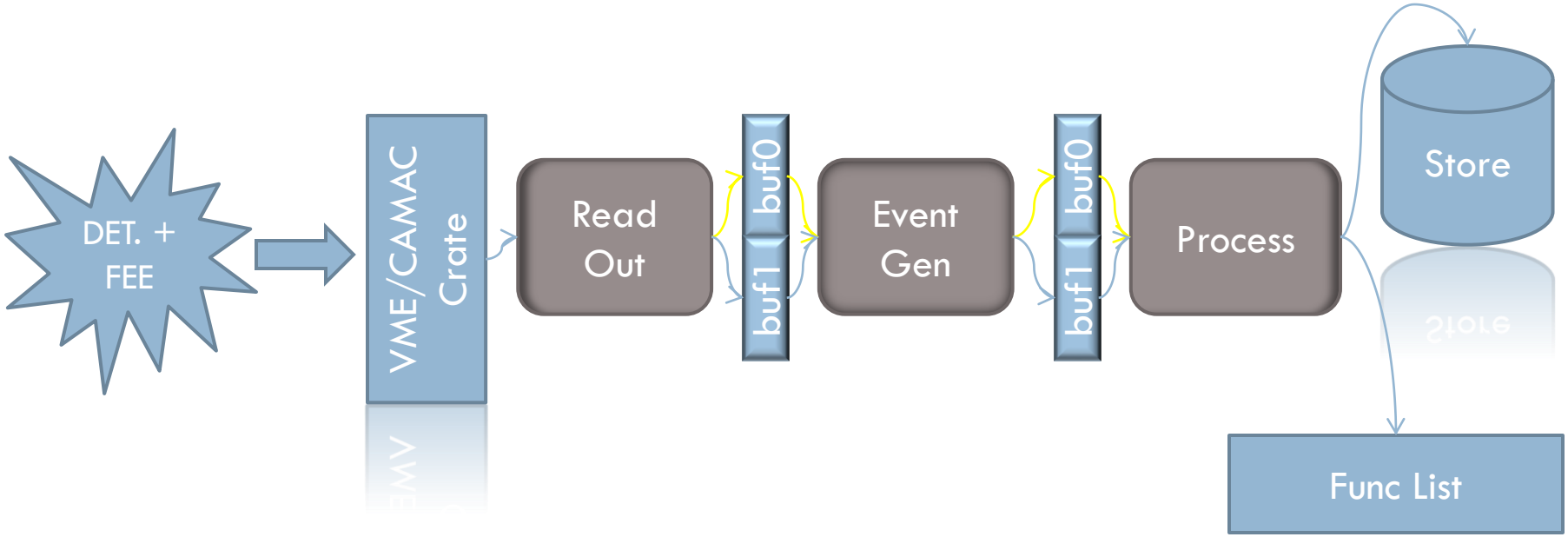
- GATE signal from Front-end electronics (FEE) is common to all
- Common Busy
- Horizontal readout in BLT or CBLT
- Block transfer and chained block transfer (32 bits)

Common dead time mode



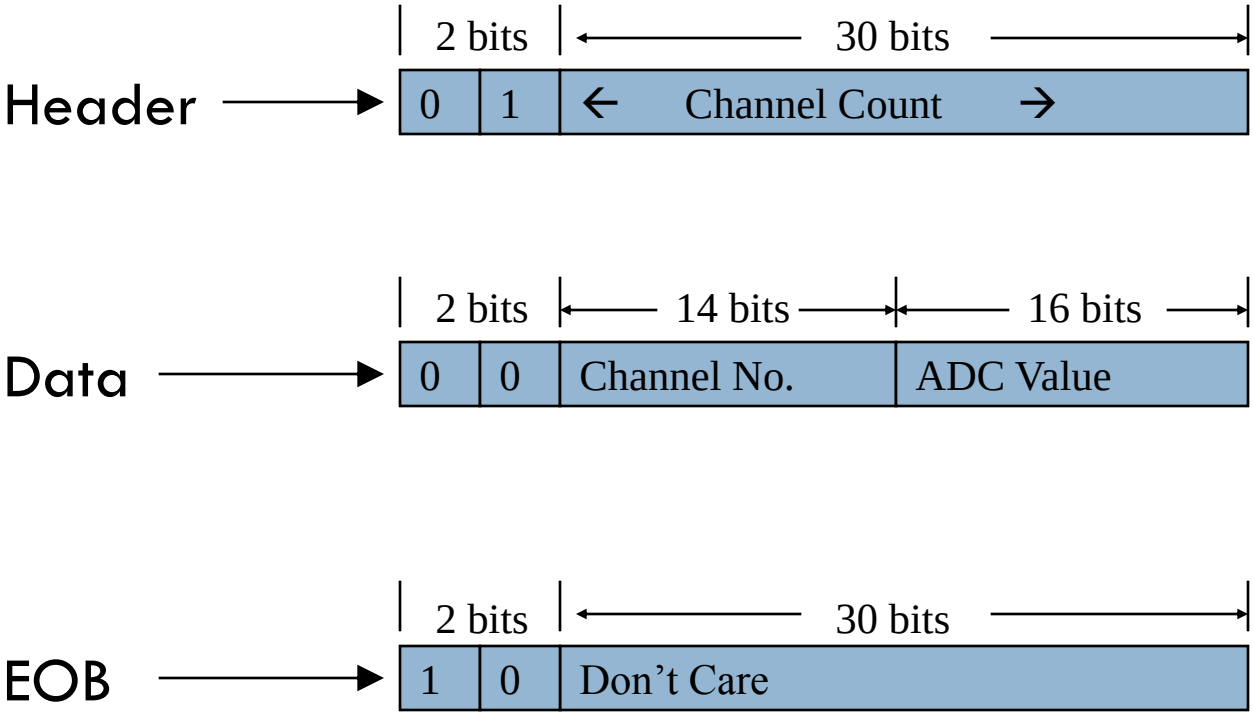
$$\tau = \underset{i=1to3}{MAX}\left(\tau_{1i} + \tau_{2i} + \tau_3 + \tau_4\right)$$

Multi-threaded Dataflow



Event structure

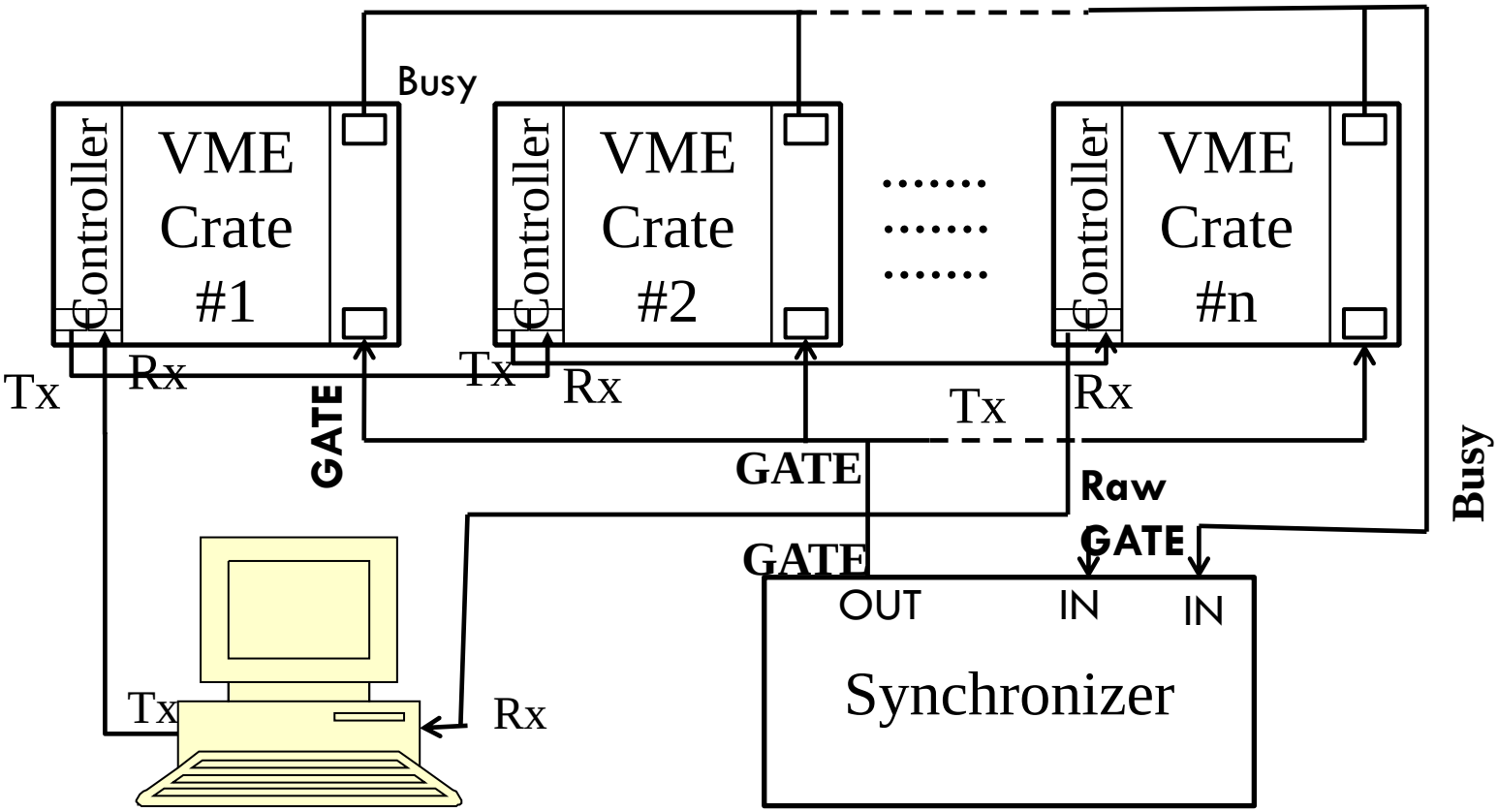
Zero-suppressed Event format



Multi-crate DAQ

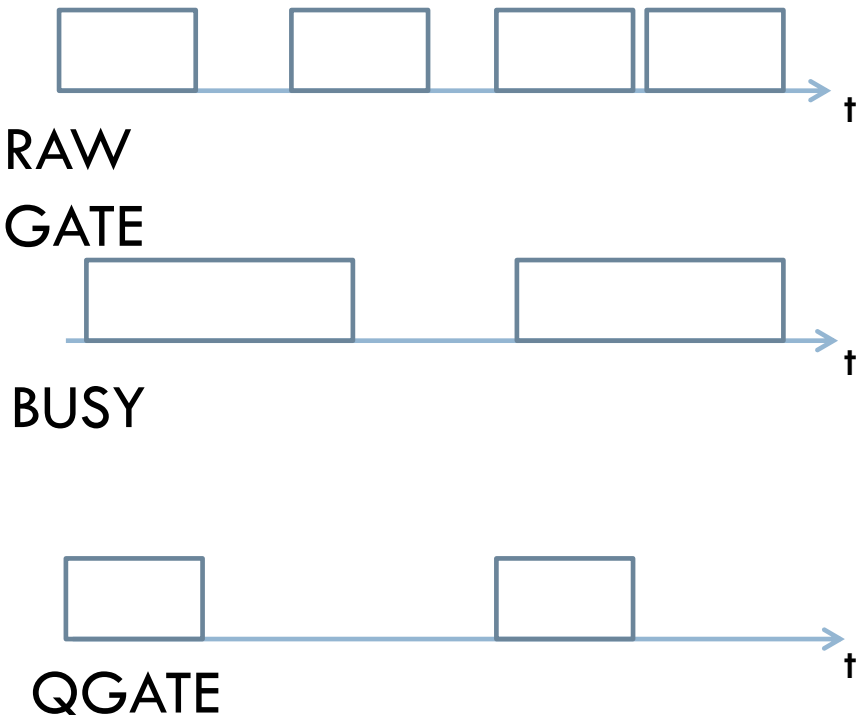
- CAEN V2718 Controller with PCI interface and fiber optics cable
- 8 crates can be daisy chained with a single interface card
- Automatic CBLT setup for individual crates
- Synchronization is done by the custom built synchronizer module.
- Common dead time mode of operation
- 1.2Mparameter/sec throughput

Multicrate VME setup



Multi crate connection

Synchronization



Timing diagram of synchronizer

- The RAW GATE is completely blocked, when the BUSY is high
- GATE signal already present at the time of busy withdrawal is also blocked.
- The width of the RAW GATE signal is always preserved.

Custom built Synchronizer module

- NIM standard module
- NIM/TTL/ECL busy input
- NIM/TTL Gate input
- NIM/TTL/ECL Gate Output
- Module blocks all the gates in busy period and always preserves the gate width
- The module can be used for multi-crate synchronization

Future plan

- FPGA based DAQ board
  - 100-125MSPS sampling ADC 12bit or more
  - Digital filter on FPGA for signal processing; replacing analog FEE modules
  - Automatic peak finding
- Heterogeneous DAQ system
  - Multiple independent DAQ (CAMAC, VME, Digital, Networked etc)
  - Absolute timestamping
- ASIC based FEE card with FPGA interface is also being explored for future upgradation

Conclusion

- CAMAC & VME based DAQ both on Linux and WindowsXP/2003 is available
- Multicrate VME version will support large number of detectors channels
- Timestamping module design and heterogeneous DAQ project has been taken up for current plan period
- Prototype development for Digital filter based DAQ board is under development

Thank you