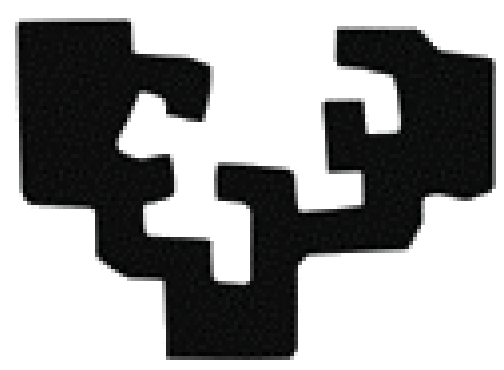


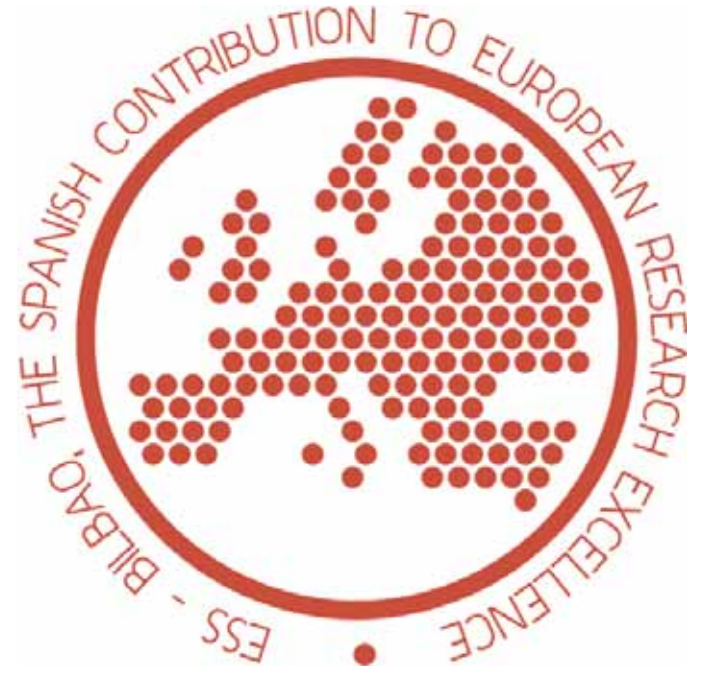
INTRODUCTION OF NONSTANDARD EPICS CONTROLLERS

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Introduction

Although EPICS is a mature software framework, the study and validation of new configurations of EPICS systems is very valuable, since new ideas open its evolution and improvement. Therefore, **the goal of the present work is to introduce new technologies under EPICS control structures and test different configurations with innovative hardware** in this kind of applications. Specifically, it is intended to validate the use of non-standard EPICS controllers. This paper presents a testbench using LabVIEW together with EPICS. LabVIEW eases and speeds up the development of control structures, avoids the hardware dependent developing costs and offers almost absolute compatibility with a high variety of hardware devices used in control and data acquisition. To validate its use in a real environment, is mandatory to make a study facing this solution and EPICS standard methodology, specifically CODAC system used in ITER. With such objective in mind, a testbench is implemented running both configurations and its results are compared. Following this scheme, as conclusions, the next step must be to implement exactly the same hardware-level structure for both approaches to improve the comparison.

Experimental Setup

The setup implements a reduced local controller, which includes data acquisition, sequencing and control. The typical signals involved in a local controller are present in the emulated system. These signals are the Process Variables (PVs) of the EPICS system. The complete set of signals consists of 1960 PVs: 400 binary inputs, 400 analog inputs and 400 calculation type PVs for each approach.

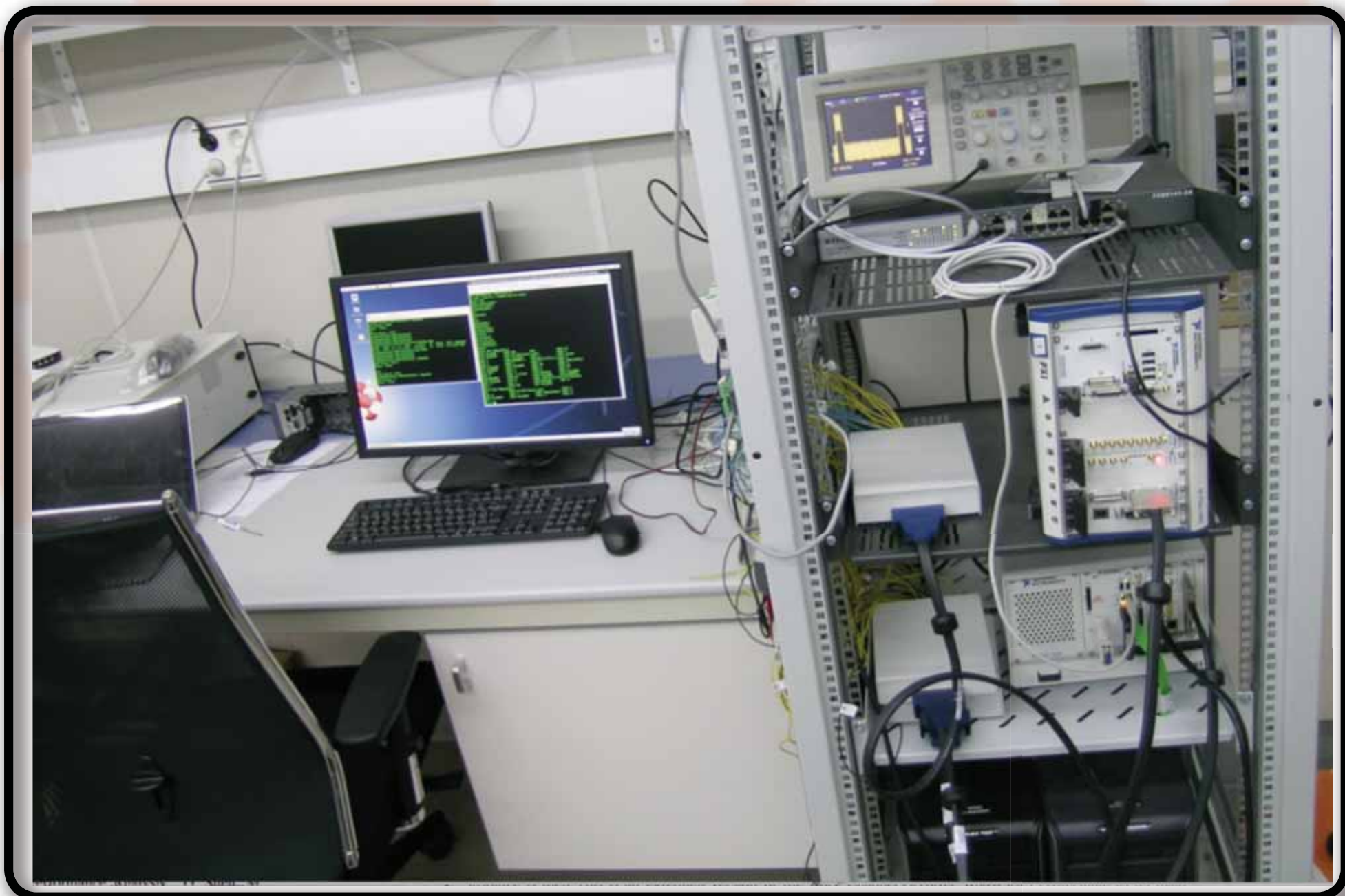


Figure II: Overview of the laboratory testbench, where both PXIs and the archiving computers are shown placed in a rack.

- The first setup is taken as a reference. The IOC is running in a NI PXI-8106 embedded controller with Scientific Linux 6 in a NI PXI 1031 chassis. A NI PXI-6259 DAQ card performs I/O tasks. As explained before, this device requires its own driver, for both Linux (SL6) and EPICS. They can be found in the ITER CODAC Core System v3.0 public version. A plant, simulating a DC motor, is implemented as Hardware in the Loop (HIL) using NI PXI-7833R multifunction card, which includes a Virtex II FPGA. The IOC database is defined including all the system PVs and their behavior.

- The second hardware setup consists of a PXI chassis from National Instruments (PXIe-1082) with a PXIe8108 controller running LabVIEW Real-Time operating system. The control actions are defined in a LabVIEW program running in the PXI controller as well as the I/O signal set. These are written into shared variables. LabVIEW also acts as an EPICS server through the EPICS IO Server for LabVIEW, which publishes desired control signals to an EPICS network via Channel Access protocol. This method allows the developer to focus on the control without worrying about drivers.

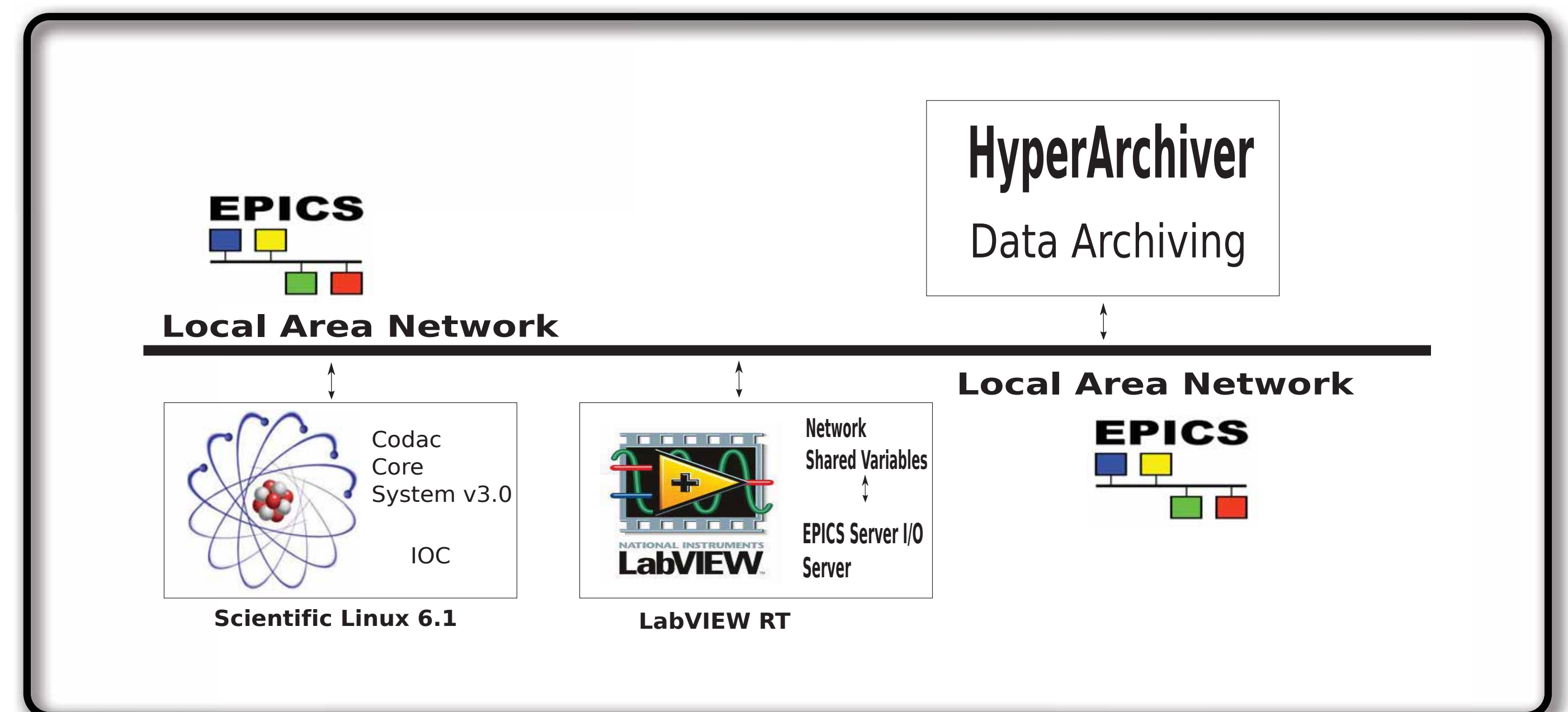


Figure I: Overall system description over the network including the two systems (LabVIEW based approach and CODAC based) to be tested and the archiving system.

LabVIEW approach	EPICS classical
PXIe-1082 Chassis	PXI-1031 Chassis
PXIe-8108 Controller	PXI-8106 Controller
2.53 GHz Intel Core 2 Duo	2.16 GHz Intel Core 2 Duo
1 GB RAM	512 MB RAM
LabVIEW RT	Scientific Linux 6.1
LabVIEW 2010 SPI	EPICS R3.14.12.2

Table I: main hardware and software settings of both test stands.

Results

All the processed data of both systems is archived in a database for a further study. In this work, a HyperArchiver instance is used. This is an extended version of the RBD Channel Archiver which uses Hypertable as its main database. The version of Hypertable used in ESS Bilbao is a modified version of the original release adapted to efficiently manage arrays of variables.

Preliminary data analysis shows similar data losses in both systems, but they seem to be consequence of the non-optimal testbench implementation (archiving and network). However, those are not EPICS-related errors, which is working flawlessly in both approaches.

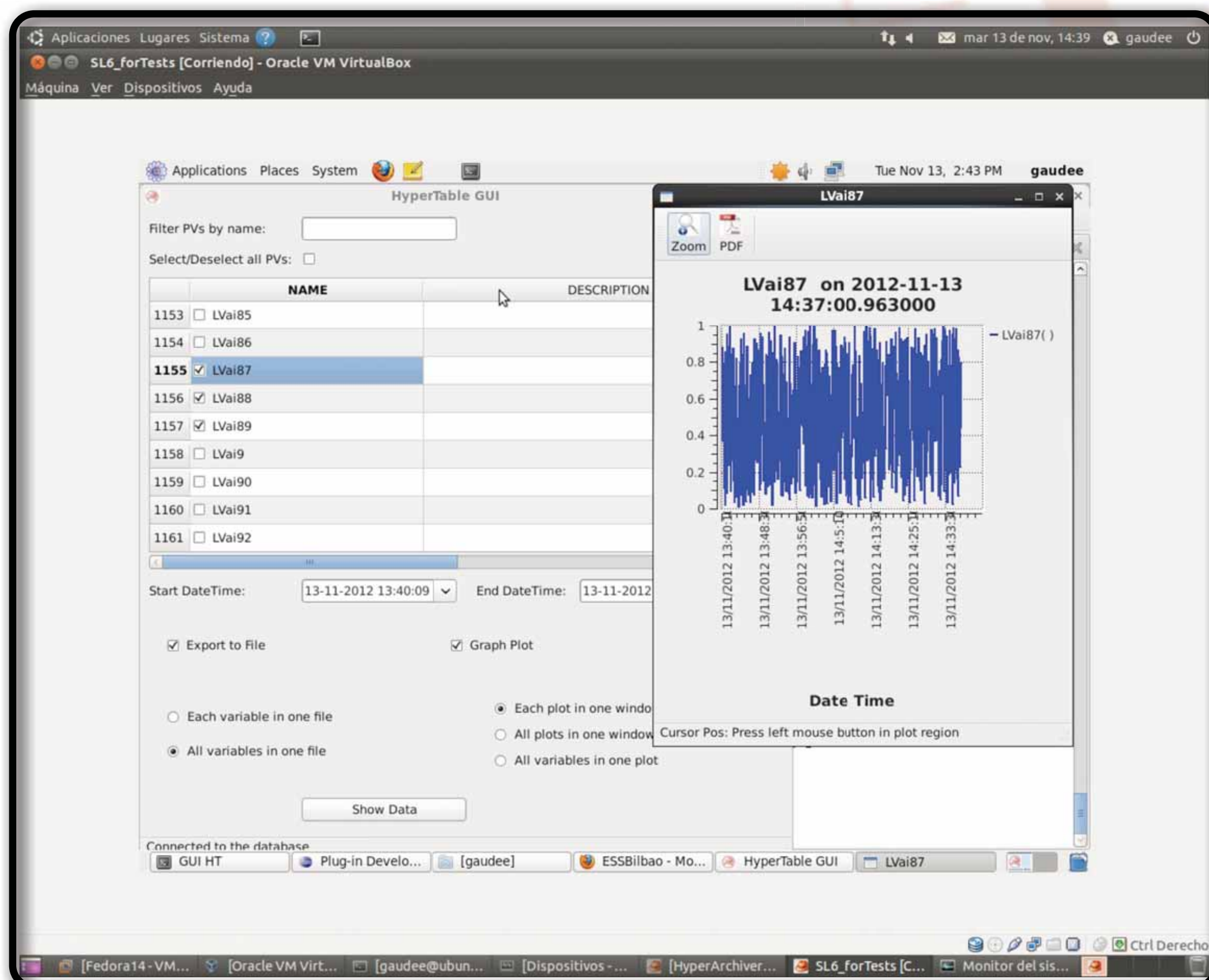


Figure III: GUI for data retrieval based on python and developed at ESS Bilbao. The picture shows a graph plot of an analog input type PV from the LabVIEW approach in a 60 minute time period.

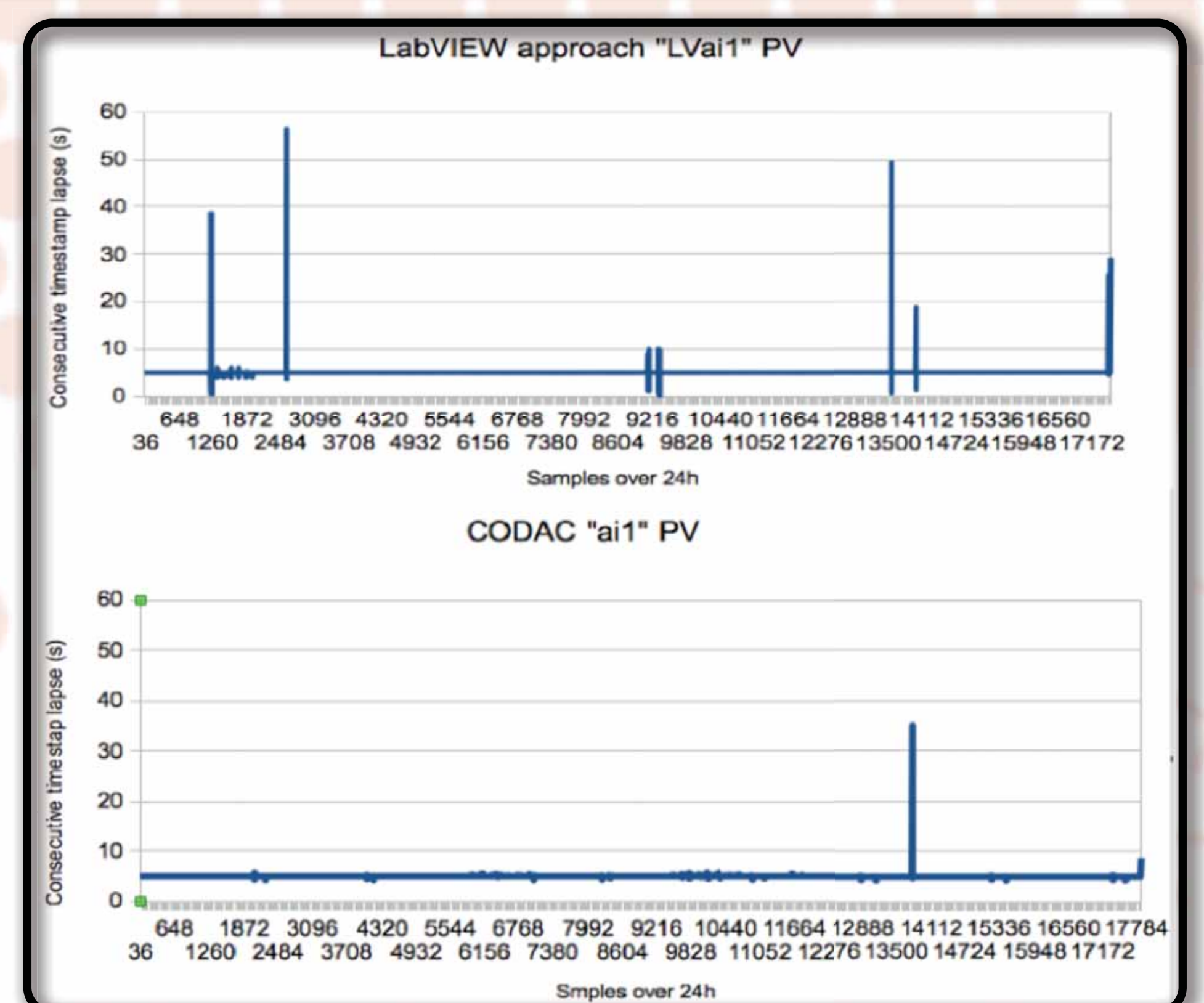


Figure IV: Graphs showing consecutive timestamp lapses of two variables, corresponding to each system. A 5s value means that no monitor is missed, while 55s indicates that 10 monitors are lost.

Future upgrades

The following upgrades are planned to implement in order to improve experimental results:

- Identical architecture: same hardware components and equal signal set acquired from a single source.
- Long term results: the testbench will run for a long time periods in order to get more reliable results and be able to conclude its applicability to real world usage.
- Synchronization over network environment using NTP like protocols.
- Addition of EPICS-based wireless links with the aim to study new monitorization architectures.