# CLIENT SERVER ARCHITECTURE BASED EMBEDDED DATA ACQUISITION SYSTEM ON PC104

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#### Abstract

The data acquisition system is designed on embedded PC104 platform Single Board Computer (SBC) with running Windows XP Embedded operating system. This is a multi channel system which consists of 12 Bit, 10 MSPS Analog to Digital Converters with on board FIFO memory for each channel. The digital control and PC104 bus interface logic are implemented using Very High Speed Hardware Description Language (VHDL) on Complex Programmable Logic Device (CPLD). The system has provision of software, manual as well as isolated remote trigger option. The Client Server based application is developed using National Instrument CVI for remote continuous and single shot data acquisition for basic plasma physics experiments. The software application has features of remote settings of sampling rate, selection of operation mode, data analysis using plot and zoom features. The embedded hardware platform can be configured to be used in different way according to the physics experiment requirement by different top level software architecture. The system is tested for different physics experiments. The detailed hardware and software design, development and testing results are discussed in the paper.

# **INTRODUCTION**

The main objective to develop this system is to provide PC based simple and easy solution for low channel data acquisition requirement to support the basic physics experiments carried out by the students. These experiments often require few channels with high sampling rate with short acquisition time. To avoid using high end resources for data acquisition application for small experiments, the system is developed which requires very minimum resources and knowledge to operate it. The Client Server architecture based embedded data acquisition system is developed on PC104 [1][2] platform which houses inside standard industrial 6U, 16T enclosure which requires minimum space to install and operate. As far as resources concerned, It requires only Ethernet local area network connectivity for full fledge operation. The basic data acquisition hardware consists of 5 channels with simultaneous sampling pipelined ADCs, which are capable of doing sampling from 1Khz to 10MHz. Each channel consists of 64K location of FIFO memory. The hardware design is very flexible and all data acquisition parameters are software controlled. The system can be operated in manual as well as external trigger mode and it also accepts external clock. The basic system level operational block diagram is shown in Figure 1.

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Figure 1: Basic system block diagram.

## HARDWARE

This embedded board is designed and assembled inhouse and it contains PC104 based Single Board Computer which is procured commercially. The designed and developed board contains analog, digital and mixed signal components. The board is designed and fabricated on four layered PCB. The hardware level block diagram and the selected components are shown in Figure 2.

- Analog front end is designed with AD524 [3] high bandwidth Instrumentation Amplifier followed by AD8041 high speed ADC driver which translates the signal level to dynamic signal range of pipelined ADC AD9220.
- Each channel contains dedicated FIFO memory of size 64K which has total three memory status flags i.e. half, full and empty which can be used for status monitoring and control purpose.
- All digital operational logic like hardware initialization, clock control, ADC and memory control, PC104 bus signal decoding are implemented in Xilinx Complex Programmable Logic Deive (CPLD), which is written in VHDL.
- The acquisition module supports internal as well as isolated external clock and trigger.
- The system contains Advantech make PCM-3353F [4] Single Board Computer which runs on Windows XP Embedded Operating System installed on 4GB size of compact flash card.



Figure 2: Basic hardware block diagram.

#### **SOFTWARE**

The client server architecture is the most suitable for this type of application, as it requires minimum installations at client side and uses local area network for data exchange. It also supports remote controlled operation which is our prime requirement.

The software development is done in National Instrument's LabWindows/CVI [5] which is ANSI C based development environment on windows platform which also provides good support for graphical user interface (GUI) development.

The LabWindows/CVI TCP Support Library provides easy-to-use callback functions to create TCP server and client applications, which are shown in Figure 3. The Callback functions provide the mechanism for receiving notification of connection initiation, connection termination, and data availability.



Figure 3: LabWindows/CVI TCP support functions.

24

## APPLICATION

The software development is divided in main two parts server application and client application. The custom protocol is designed using the data packets, which are exchanged between server and client application to establish the operation, control and status monitoring of the embedded hardware.

#### Server Application

The Server application runs on the embedded hardware platform and it mainly controls the hardware parameters of the module depending on user inputs provided through client application running on remote networked machine. Server application generates the control commands and reads the status of the hardware through PC104 bus. The generated PC104 bus signals are decoded by the firmware implemented on CPLD and it generates the low level hardware signals as shown in table 1

Table 1: PC104 Address Decoding

PC104 Address	Decoding
0x306,0x308,0x30A, 0x30C,0x30E	16 bit read cycle for each channel data read out(read)
0x301	FIFO Reset (write)
0x302	FIFO Clock Enable (write)
0x303	Trigger Status (read)
0x304	Trigger Mode (write)
0x305	Clock setting (write)
0x309	Half Flag Status (write)

The GUI of server application is shown in Figure 4. The connections details and the commands received from the client application are displayed in the text boxes. After decoding the command, the server application sets the hardware parameters and the status is indicated on the panel in form of illuminated leds.

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- New connection from 192.1 110491020910309101	68.201.78	<u> </u>	Clock Sele
- New connection from 192.1 110491020910309101 - Online - 🎲	68.201.78	4	Clock Sele
- New connection from 192.1 10491020910309101 - Online - 🎲	68.201.78	4	Clock Sele Initialise
- New connection from 192.1 10491020910309101 - Online	68.201.78		Clock Sele
New connection from 192.1 10491020910309101 -Online - 🌑 Server IP: 192.168.204.133 Server Name:	68.201.78 Connected: Client IP: 192.168.201.78 Client Name:	*	Clock Sele

Figure 4: Server application GUI.



Figure 5: Client application GUI with acquired data.

## **Client** Application

The client application runs on any networked computer and it remotely controls the embedded data acquisition system. The GUI of client application is shown in Figure 5. It supports plotting of all channels and some basic data analysis utilities like zoom, restore and plotting from files.

After successful connection with server, all the parameter settings buttons are activated through which user can set the data acquisition parameters of the embedded system. These are embedded in the data packets with the starting string number '91' followed by the data parameter. After completion of the data acquisition, the server application transfer the data of each channel which are received by the client application and stored in the file based database for particular defined shot number. The proper reception of the file is indicated in the receive text box with the starting string number '92' which is sent by the server application and followed by the channel number. The connection details and the acquired data are shown in Figure 5.

The assembled and tested system with all components is shown in Figure 6.

## ACKNOWLEDGMENT

The authors sincerely expresses thanks to all the members of Electronics Group.



Figure 6: Embedded Data Acquisition System.

## REFERENCES

- Y. Guozhen, S. Qiufeng, L. Li, "Design of electric power data acquisition card based on PC/104 bus", International Conference on Electrical and Control Engineering-2010 (ICECE 2010), pp. 5130–5133.
- [2] PC/104 Consortium; http://www.pc104.org
- [3] http://www.analog.com
- [4] http://www.advantech.in
- [5] http://www.ni.com

ISBN 978-3-95450-124-3