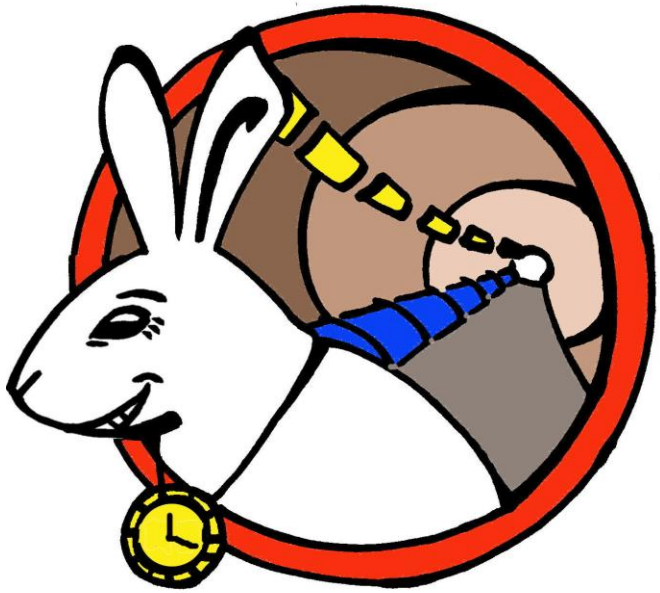


The WhiteRabbit Timing System

M. Kreider,
T. Fleck

WhiteRabbit is designed to do...

- Time Synchronisation
- Timestamping
- Machine Control
- Deterministic Switching

WhiteRabbit offers...

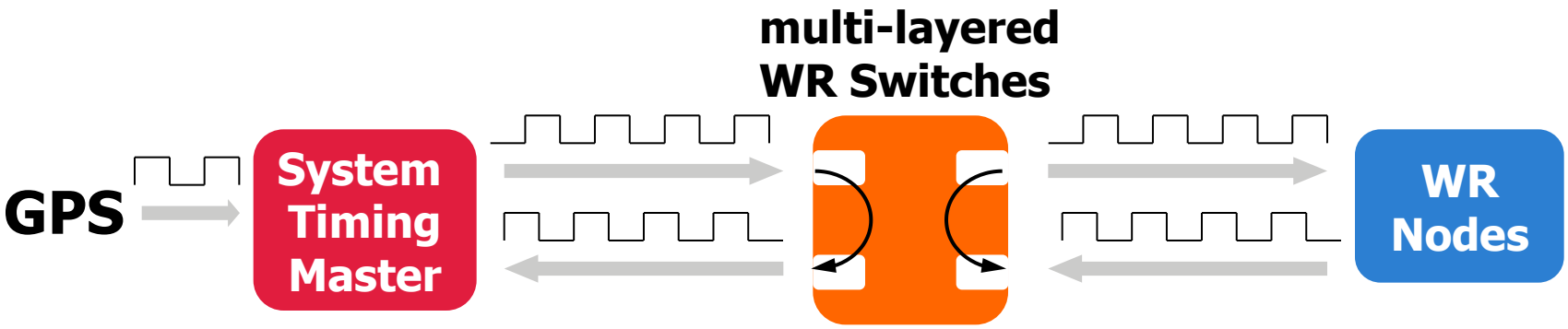
- Timing Accuracy: < 1ns, < 20ps Jitter
- Robustness: event loss < 10^{-12}
- Scalability: 2000 timing receivers
- Link length: up to 10 km

WhiteRabbit employs ...

- PTP – Precision Timing Protocol
- QoS – Quality of Service
- FEC – Forward Error Correction

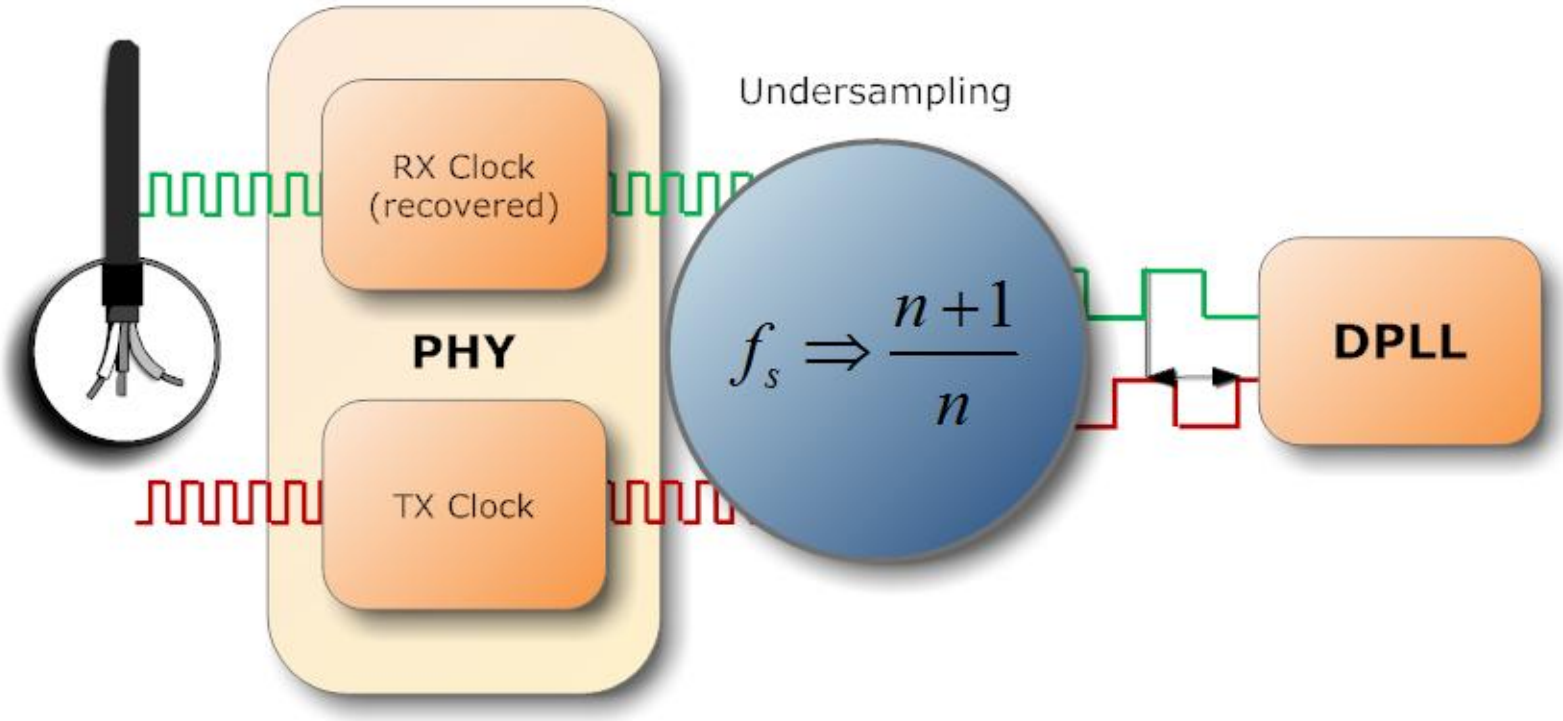
SyncE: One clock is enough

- Nodes use same physical clock
- Clock encoded in Ethernet carrier
- Clock recovered by PHY PLL


multi-layered
WR Switches
GPS
System
Timing
Master
WR
Nodes

Precise Phase Measurement – Aiming for Accuracy

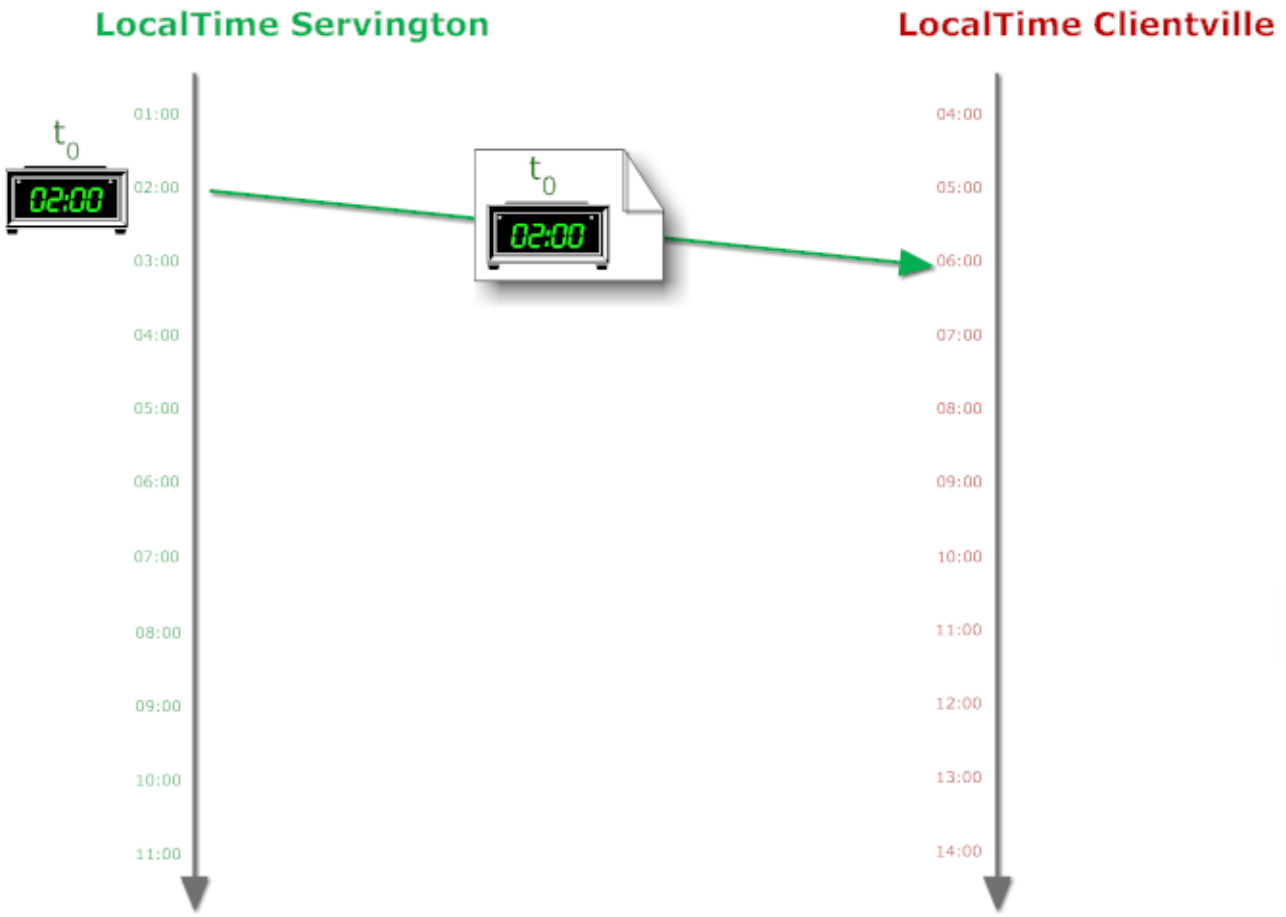
- Undersample Clocks
- Feed resulting alias frequencies to PLL
- Determine phase difference


Undersampling
RX Clock
(recovered)
PHY
TX Clock
$f_s \Rightarrow \frac{n+1}{n}$
DPLL

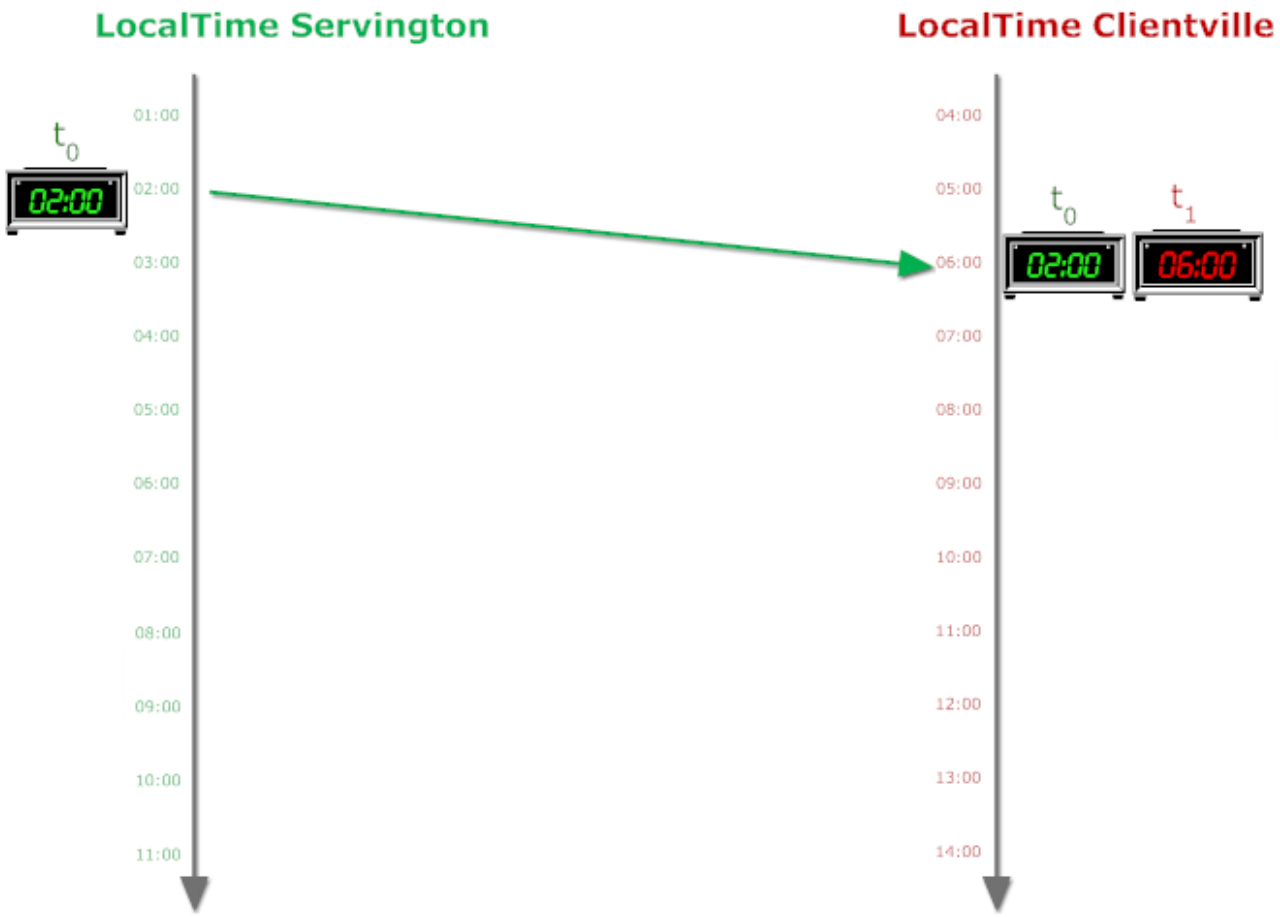
PTP – Time Sync at a Handshake

- Exchange messages between nodes
- Timestamp Msg arrivals and departures
- Calculate link delay and time difference
- Share results, adjust client clock

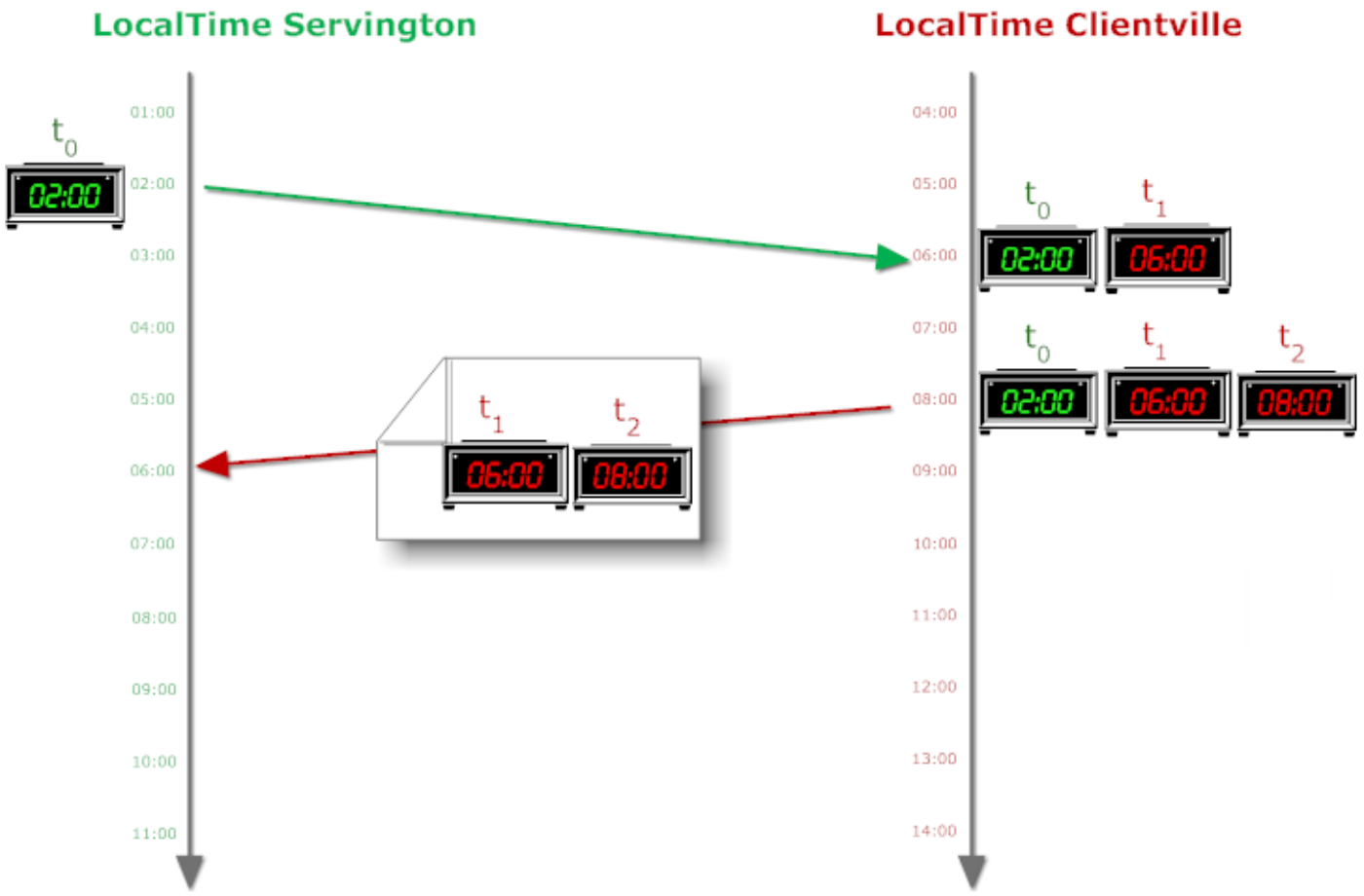
PTP – A Simplified Example



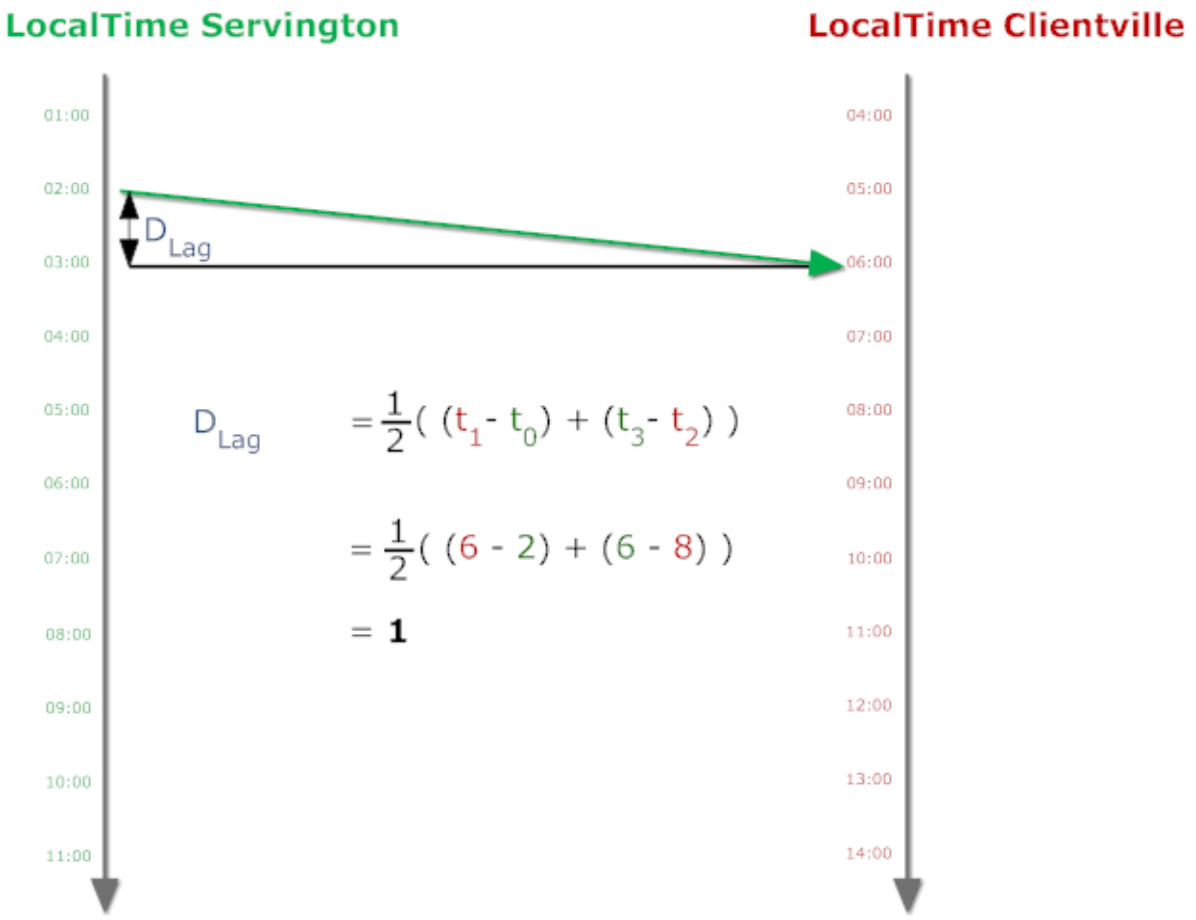
PTP – A Simplified Example



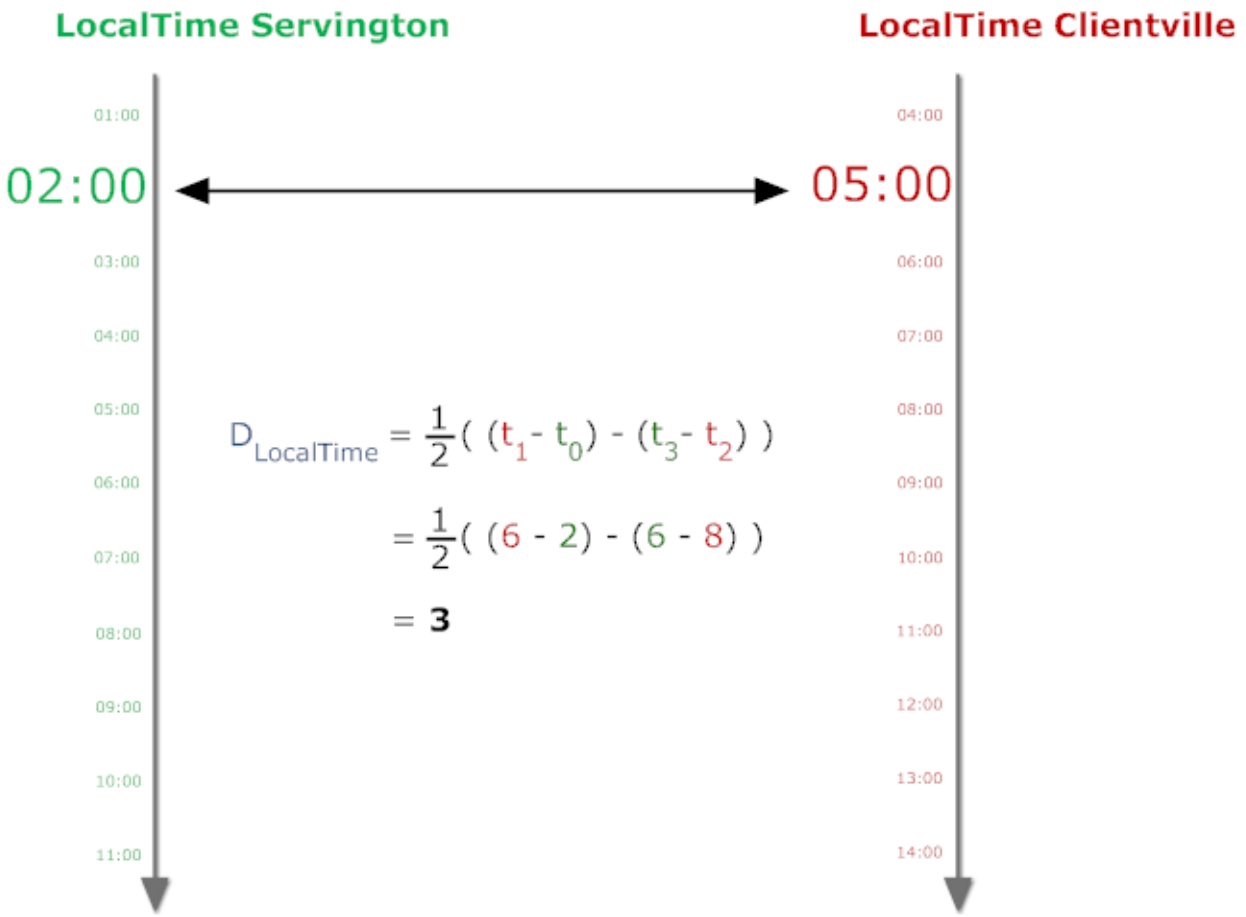
PTP – A Simplified Example



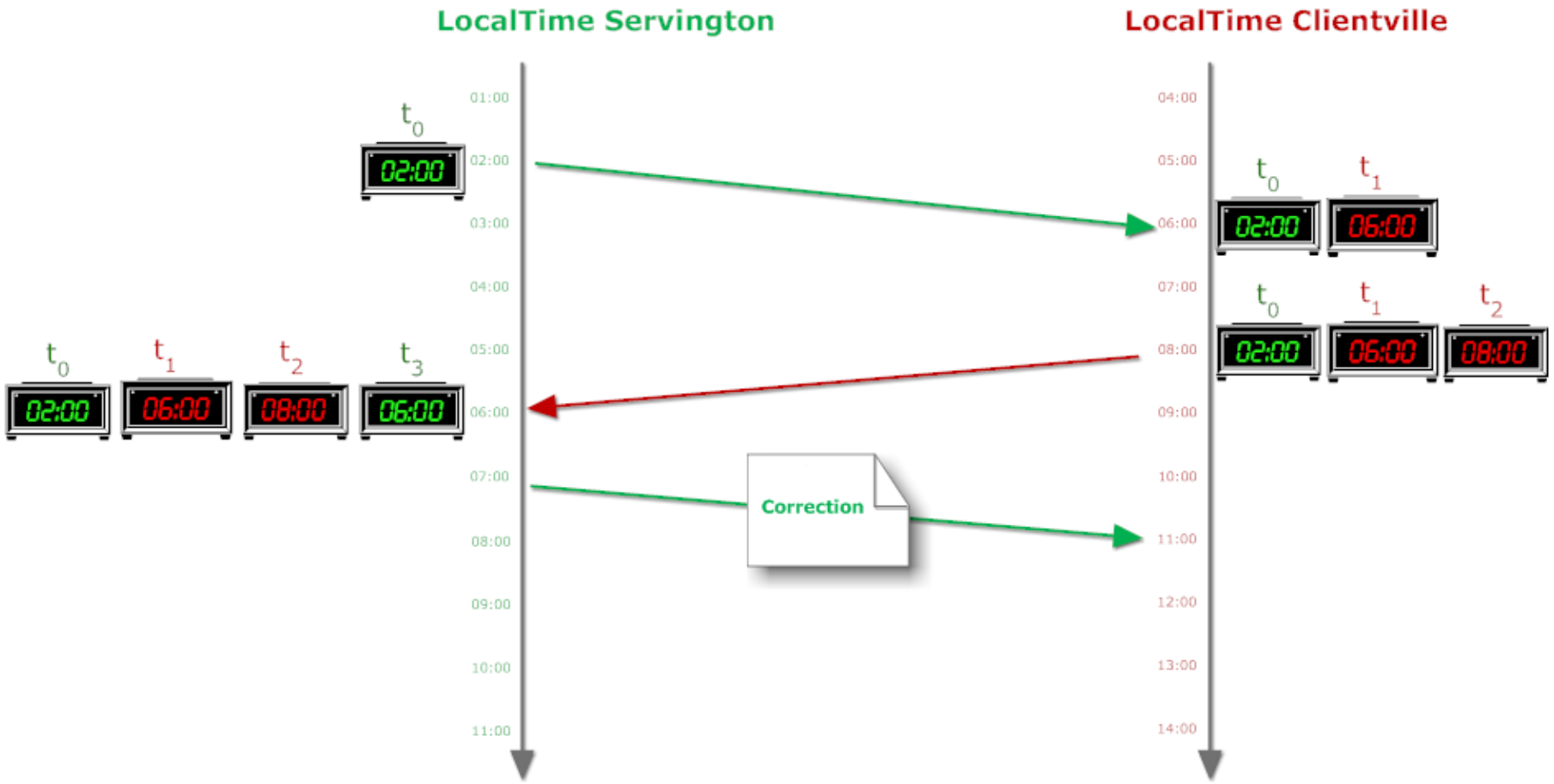
PTP – A Simplified Example


LocalTime Servington
LocalTime Clientville
01:00
02:00
03:00
04:00
05:00
06:00
07:00
08:00
09:00
10:00
11:00
04:00
05:00
06:00
07:00
08:00
09:00
10:00
11:00
12:00
13:00
14:00
D Lag
D Lag = ½((t1 - t0) + (t3 - t2))
= ½((6 - 2) + (6 - 8))
= 1

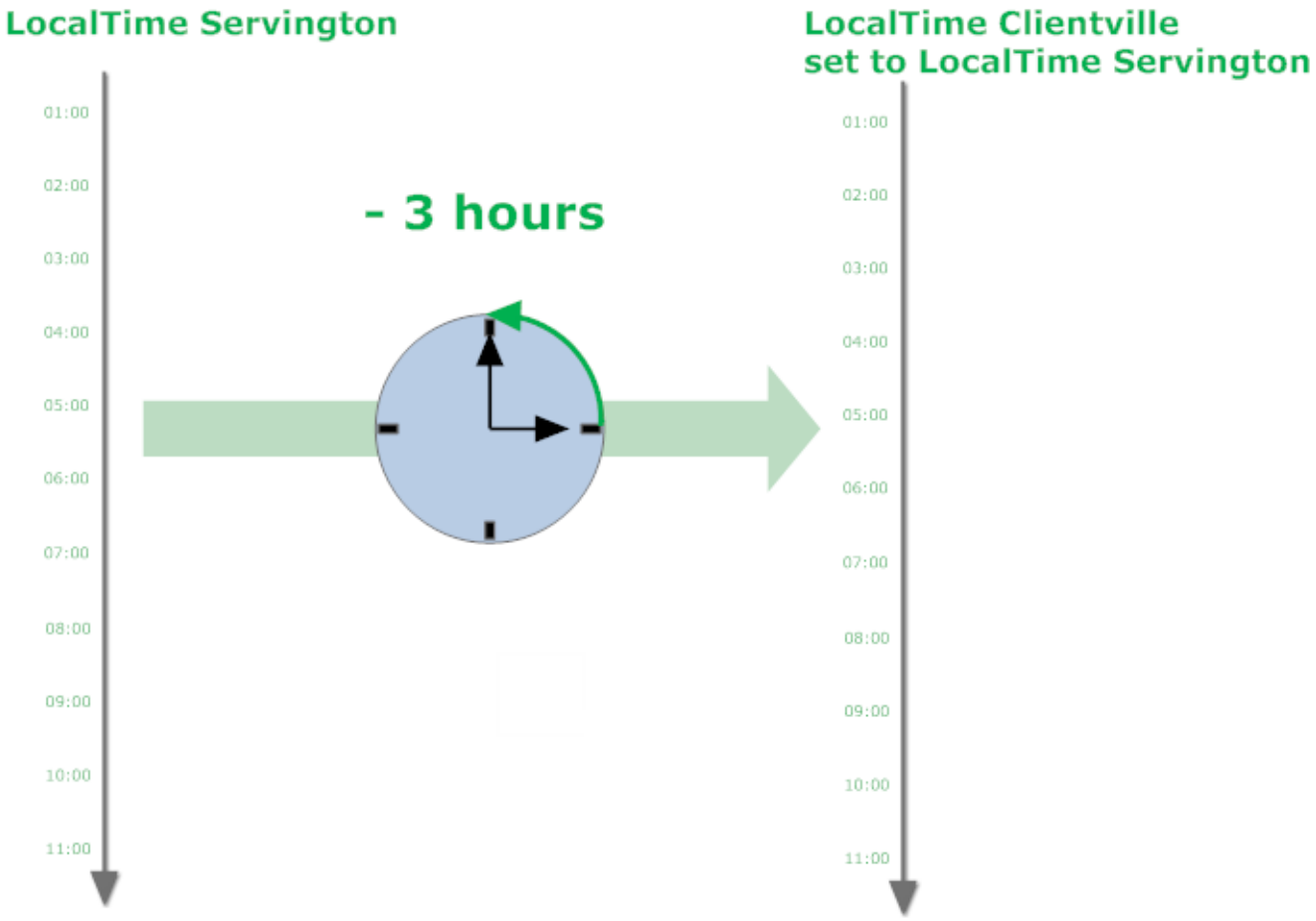
PTP – A Simplified Example



PTP – A Simplified Example



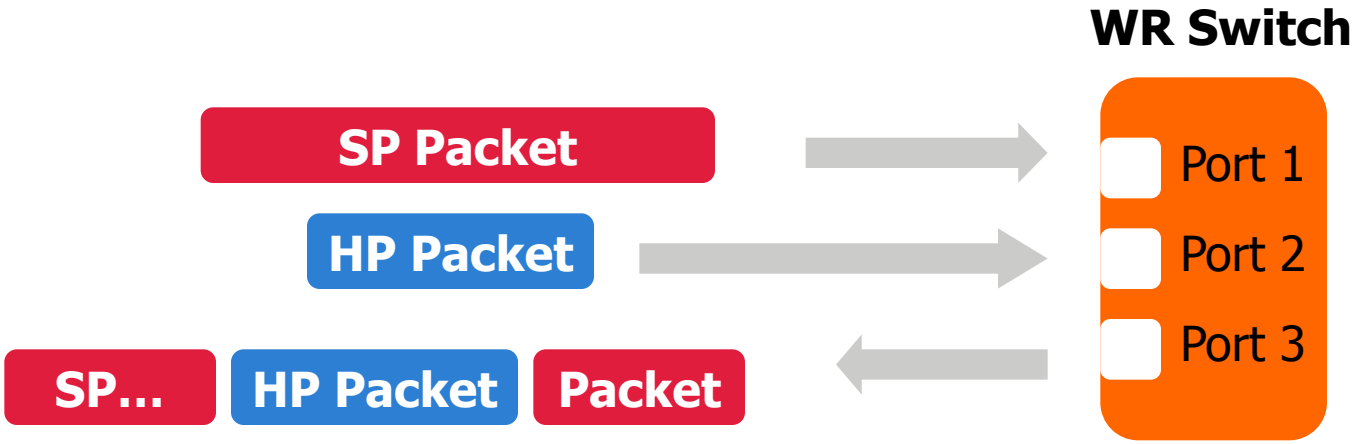
PTP – A Simplified Example



QoS – Not all packets were created equal

- Ethernet traffic split into:
  High **P**riority (**HP**) packets
  Standard **P**riority (**SP**) packets

- HP packets can preempt other packets „on-the-fly”


WR Switch
SP Packet
HP Packet
SP...
HP Packet
Packet
Port 1
Port 2
Port 3

Timing Master – Telling everyone what to do

- Generate Event Sequences
- Powerful CPU
- Real Time Parallel Scheduling in FPGA
- Granularity Window for Load Balancing

Where WhiteRabbit is now:

- Functional high precision Time Sync since 2009
- FAIR Timing Master prototype under development
- Switch, master and receiver specs in progress
- WR test system first prototype complete
- WR protocol implementation under development

Where WhiteRabbit will be:

- WR switch prototype end of 2010
- Timing receiver board development in 2010-2011
- FAIR Timing Master prototype early 2011

Thank you
for your attention

Time for your Questions