

Control and Timing system design of CPHS

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Abstract—The control system consists of a timing and event distribution system, an EPICS based distributed run-time database and control system, and a comprehensive personnel and machine protection system. The timing and event distribution system defines the global system time frame as well as specific events that trigger local devices by an event generator and receiver framework, so that the time delay of each event could be controlled in 10ns resolution, and the timing jitter of trigger signal is below 0.1ns. The hard-real-time machine protection system is also integrated in the event system so that a fault event could be responded within 50 micro-seconds. Field control signals such as water temperature, vacuum, low level RF phase and amplitude and radiation dose are monitored and controlled via the EPICS database through Ethernet.

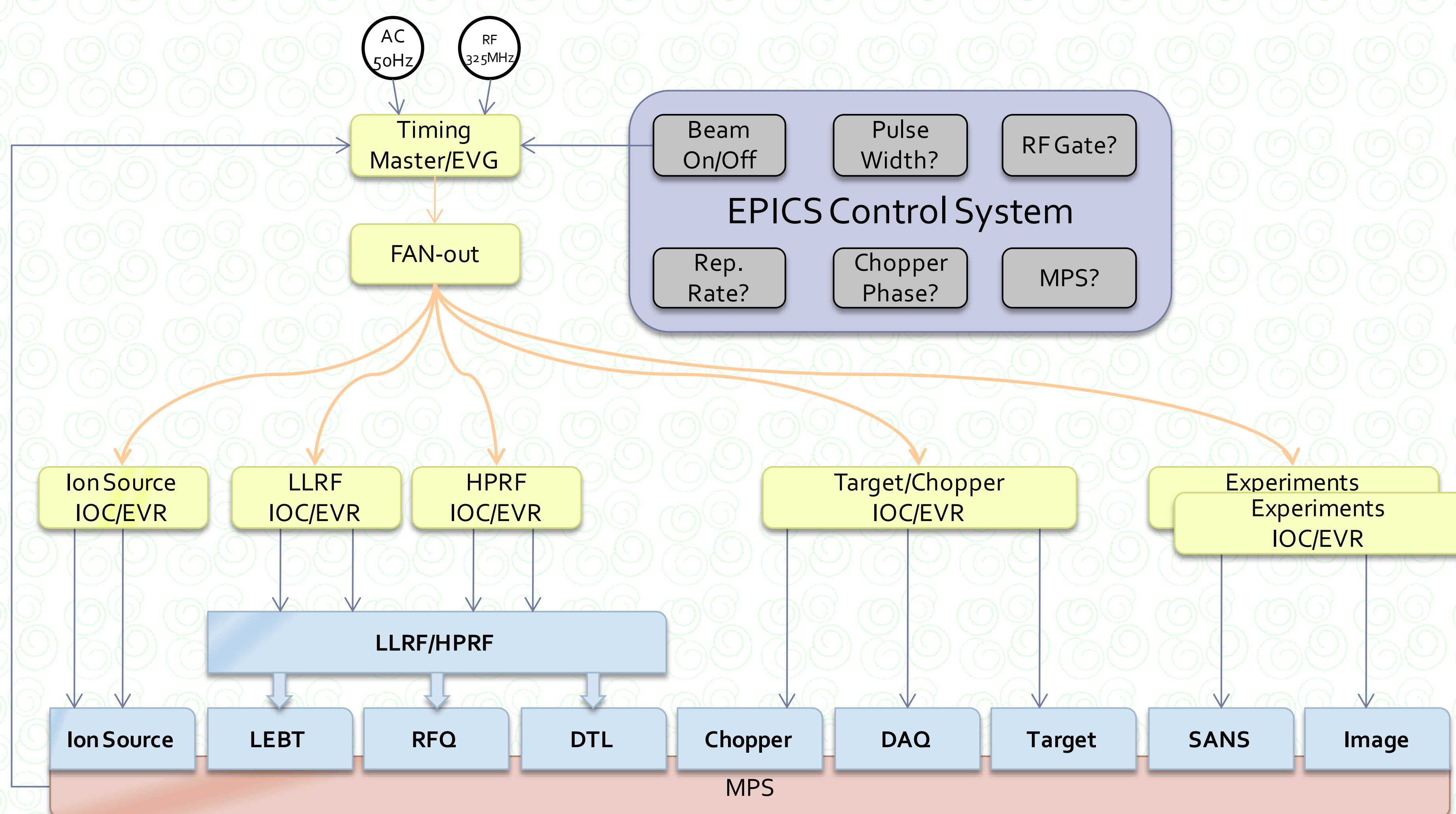


Fig 1. CPHS event distribution system

Outline—CPHS timing events are generated, encoded and distributed through optic fiber at 100MHz rate, and then decoded by different local receivers. The event receiver is integrated with an EPICS real-time IOC (RTEMS 4.9.4) so that event encoder, sequence, local delay, local trigger frequency etc. are able to be managed through any EPICS OPI.

Hardware—The Timing System consists of an Event Generator (EVG) which converts timing events and signals to an optical signal distributed through Fan-Out Units to an array of Event Receivers (EVRs). The Event Receivers decode the optical signal and produce hardware and software output signals based on the timing events. Additionally, by combining 8-bit signal simultaneously with event codes, the so-called distribution bus greatly extends the system flexibility.

EVG and EVR are commercial available CompactPCI modules from MRF Inc. (PXI EVG 230, PXI EVR 230) Local controller is NI PXI-8183.

Software—The Local IOCs with EVG and EVR are integrated with EPICS device support and applications, and every diskless IOC net-boots from CPHS DHCP server, initializes CPCI driver and loads their EPICS records. The IOC OS is RTEMS 4.9.4. The Modular Register Mapped PXI EVG/EVR driver are tested based on an extended devLib-pci with EPICS base. (<http://epics.hg.sourceforge.net/hgweb/epics/mrfioc2>)

Conclusions— The prototype of CPHS timing system with MRF PXI EVG/EVR are established and tested with EPICS-RTEMS supported. Timing performances such as delay resolution, event encoding/decoding, event sequence testing and EPICS remote access are verified.

Fig 2. Timing system configuration with EVG & EVR

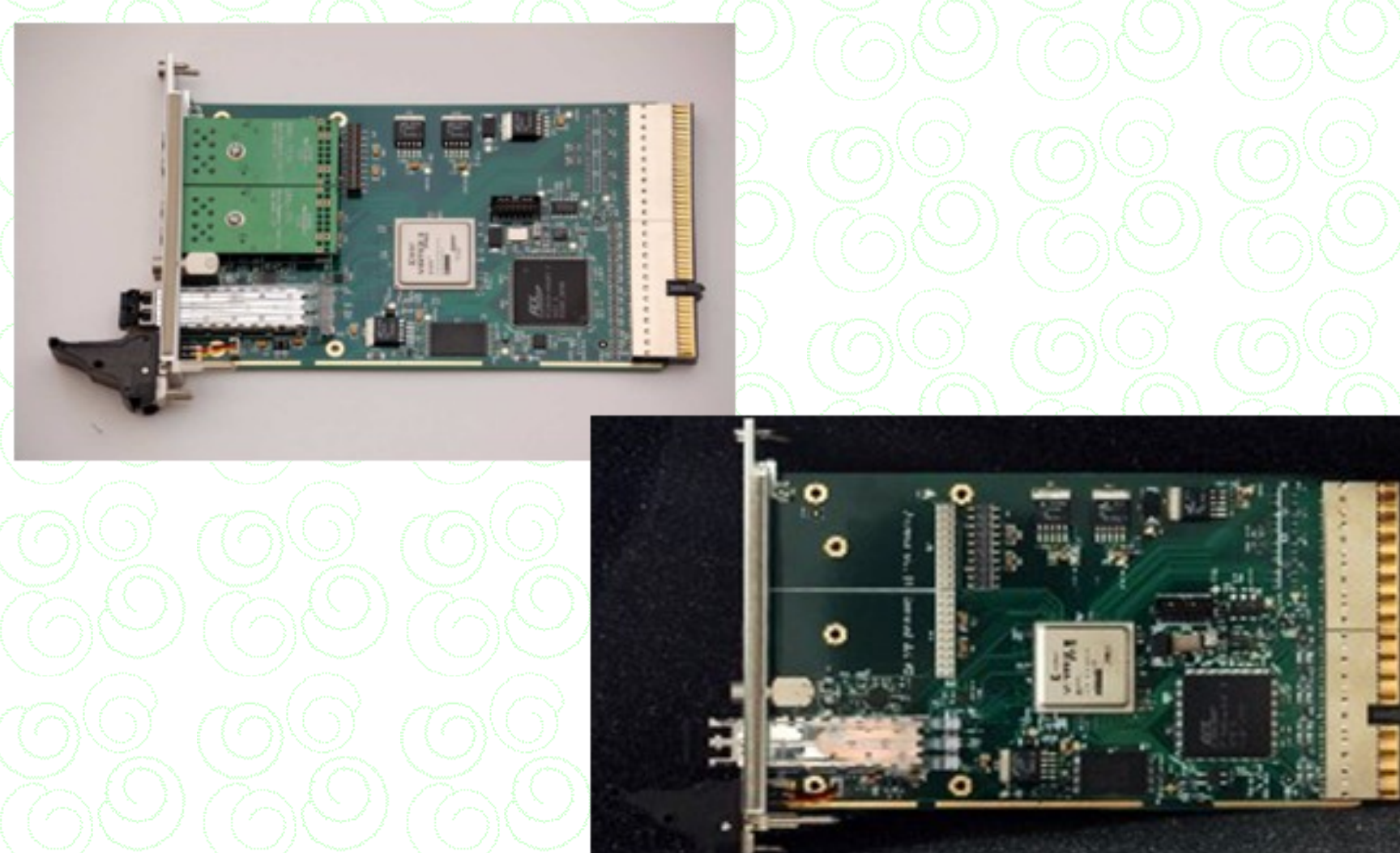


Fig 3. Event Receiver Block Diagram

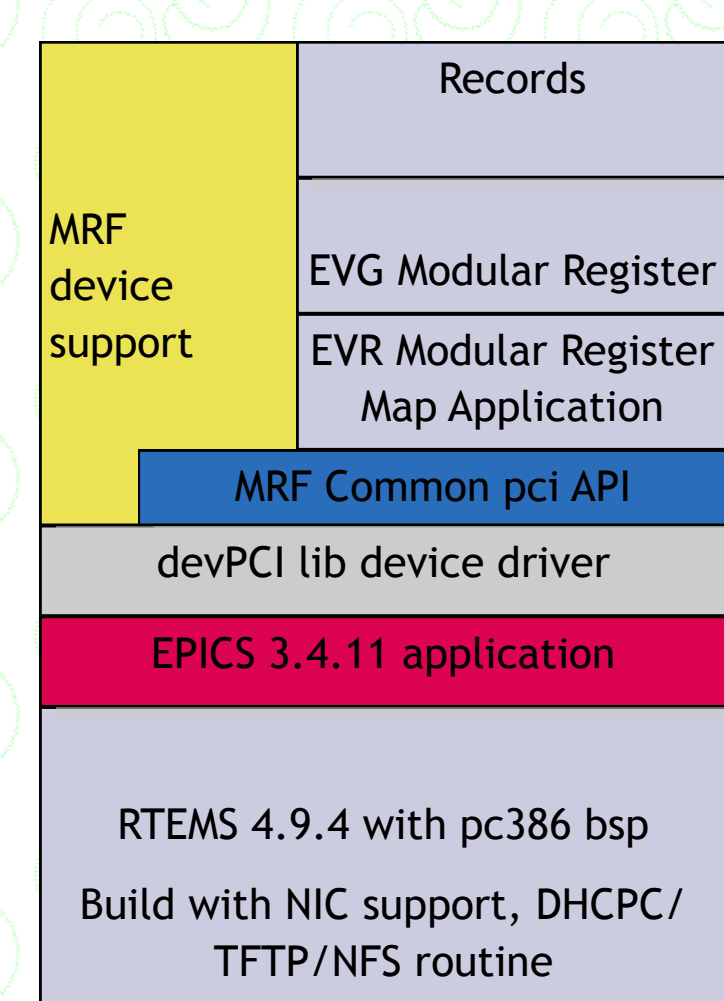
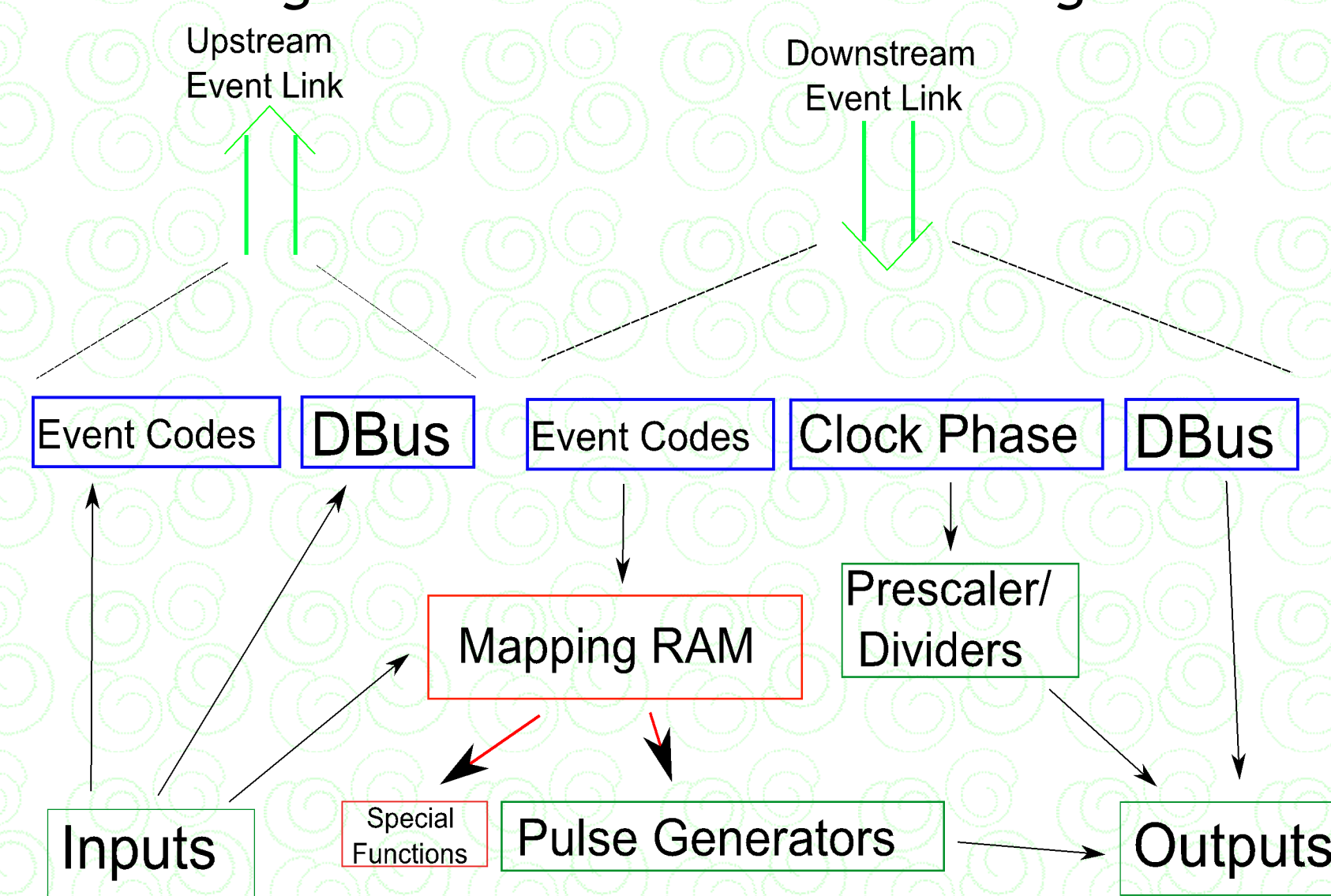


Fig 4. EVR EDM interface, and system test photo