A TWO-BUNCH BEAM POSITION MONITOR

E. Medvedko , R. Aiello, S. Smith
Stanford Linear Accelerator Center, Stanford, CA 94309, USA

Abstract

A new beam position monitor digitizer module has been designed, tested and tuned at SLAC. This module, the electron-positron beam position monitor (epBPM), measures position of single electron and positron bunches for the SLC, LINAC, PEPII injections lines and final focus. The epBPM has been designed to improve resolution of beam position measurements with respect to existing module and to speed feedback correction [1]. The required dynamic range is from 5×10^{8} to 10^{11} particles per bunch (46dB). The epBPM input signal range is from ±2.5 mV to ±500 mV. The pulse-to-pulse resolution is less than 2 μm for 5×10^{10} particles per bunch for the 12 cm long striplines, covering 30° at 9 mm radius. The epBPM module has been made in CAMAC standard, single width slot, with SLAC type timing connector. 45 modules have been fabricated.

1 INTRODUCTION

The epBPM module has four input channels X+, X-, Y+, Y- (Fig. 1), named to correspond with coordinates of four striplines - two in horizontal and two in vertical planes, processing signals to the epBPM inputs. The epBPM inputs are split for eight signal processing channels to catch two bunches, first - the positron, then the electron bunch in one cycle of measurements. The epBPM has internal and external trigger modes of operations. The internal mode has two options - with or without external timing, catching only first bunch in the untimed mode. The epBPM has an on board calibration circuit for measuring gain of the signal processing channels and for timing scan of programmable digital delays to synchronize the trigger and the epBPM input signal's peak. There is a mode for pedestal measurements. The epBPM has 3.6 μs conversion time.

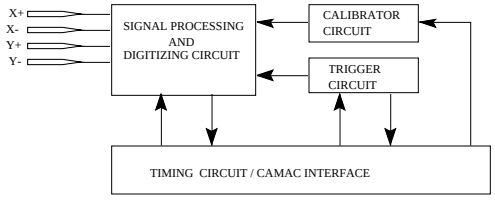

Figure 1. The epBPM module block diagram.

2. THE SIGNAL PROCESSING AND DIGITIZING CIRCUIT

The input signal from the stripline electrode "X+" propagates through the Splitter/Combiner S/C1 (5MHz - 500MHz bandwidth) and Bessel Lowpass Filter (40 MHz bandwidth) (Fig. 2). This signal goes to the Signal Amplifier (OA1, gain 5) and to the Trigger Amplifier (OA2, gain 2). The S/C2 accepts the calibration signal, S/C3 assepts signal from the stripline electrode "X-".

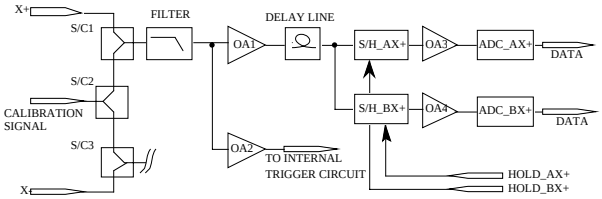

Figure 2. The Signal Processing and Digitizing Circuit - X+ channel.

The Signal Amplifier feeds a 27 ns delay line (74 MHz bandwidth). Delayed signal goes to two fast sample-and-hold amplifiers analog inputs S/H_AX+ and S/H_BX+ (14-bits accuracy, 30 ns acquisition time, ±2 mV/μs droop rate). The delay line compensates propagation delay of the S/H triggering pulse through the Trigger Circuit in order to hold the S/H input signal peak. The "A" and "B" sample-and-hold output signals go to amplifier OA3 and OA4 (gain 2), respectively. Those amplifiers narrow signal bandwidth to 4 MHz to meet ADC bandwidth (1.5 MHz). The ADC has 14 bit resolution (13 bits plus sign), 400 ns acquisition time, 2.9 μs convertion time, serial data output.

3. CALIBRATOR CIRCUIT

The Calibration Circuit generates bipolar pulses like positron or electron signals from the stipline electrode. The Calibrator is used for the signal processing channels gain measurements and for the calibration of the programmable digital delays in the trigger pulse chain.

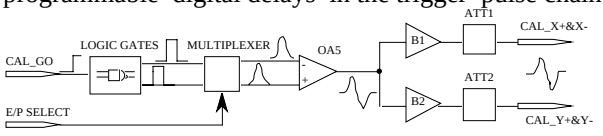

Figure 3. The Calibrator Circuit.

The calibration start pulse (CAL_GO) propagates through gates and generates two short pulses, one delayed from the other by 4 ns (Fig. 3). The multiplexer selects which pulse will be first at the differential amplifier OA5 (gain 2) inputs. If the first pulse goes to positive input and the delayed pulse goes to negative input - the OA5 output pulse will be positron-like, if the first pulse goes

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to the negative input and the delayed one - to the positive, it will be electron-like pulse. OA5 output signal feeds two buffers. The buffers output signals drive programmable attenuators, 30 dB dynamic range, both attenuators have the same input data. The Calibrator's attenuated signal supplies two S/C (channels X+, X- and Y+, Y-). The Calibrator's output signal maximum amplitude is ±1.5 Vpk-pk, 4 ns between peaks.

4. TRIGGER CIRCUIT

4.1 Trigger mode selection and timing adjustment circit

The epBPM module has three options for triggering the S/H amplifier synchronous with the epBPM input signal peak. The sources of triggering pulses are - external gates, coming from the SLAC timing distribution system, internal trigger pulse or combination of the external gate and the internal trigger pulse. Those triggering modes are called - External Trigger, Gated and No Timing. In the External trigger mode there is an option to fire a pedestal trigger pulse calibrating the zero offset of the signal processing and digitizing channels.

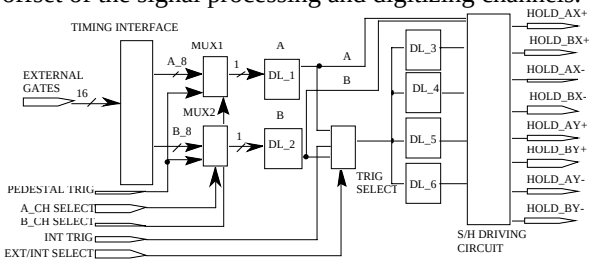

Figure 4. Trigger Circuit block diagram.

Timing interface is a 16-channels bus. The first signal (A) gate channels are 0 to 7 and the second signal (B) gate channels are 8 to 15 (Fig. 4). Multiplexers MUX1 and MUX2 select specific A and B channels respectively. MUX1 and MUX2 outputs go to trigger inputs of the programmable delays DL_1 and DL_2. The purpose of those delays is to compensate external gate cables mismatch.

DL_1 and DL_2 output signals (gate "A" and gate "B" respectively) and the internal trigger pulse go to trigger mode select gate (TRIG SELECT). The TRIG SELECT output pulse is gate "A" or gate "B" in the External Trigger mode, or internal trigger pulse in Gated or No Timing mode. The selected signal comes to the input of programmable delays DL_3 to DL_6. Delays DL_1 - DL_6 feed the S/H driving circuit, distributing inputs signals according to the selected mode of operation.

In the External Trigger mode the S/H "Hold" clock is synchronized with the external gate, in the Gated mode - with the internal trigger within the external gate, in the No Timing mode - with the internal trigger.

The signals from the Calibrator come to the S/H_A and the S/H_B at the same time. In the beam measurements the second bunch can be delayed from the first by time delays between 60 ns (minimum) and 400 ns (maximum), so the S/H_A starts to hold signal earlier, than the S/H_B. The ADCs start convertion signals for channels A and B is held off until 400 ns (ADC aquisition time) after the B channels are held. This prevents the noise due to start convertion and data clocking out pulses from corrupting the B channels data being held. After the signals convertion, all ADCs data are clock out (16 pulses, 5 MHz frequency) to the CAMAC interface registers, then the S/H driving circuit resets and the S/H amplifiers switch to sample mode.

The programmable delays DL_3 to DL_6 are used for the epBPM internal timing adjustment - to match S/H "Hold" pulse and S/H input signal peak. An individual delay is used for each signal processing channel. Calibrated delay data is stored in programmable read only memory (EPLD). Every module has individually burned EPLD. Delay data loads automatically at power on or at module reset.

The delays DL_1 to DL_6 output signal duration is 50 ns, programmable delay value could vary from 0 to 9.8 ns with 38 ps step, digital data 0 to 255 respectively.

4.2 Pedesta l trigger processing circuit

Timing channel 15 is reserved for pedestal measurements. Pedestal trigger follows the same chain as external gate. Synchronous with pedestal trigger the S/H stores the input signal value with no beam or calibrator pulse present. The ADC returns this value, which is the zero offset of the signal processing and digitizing channel.

4.3 Internal trigger circuit

The internal trigger pulse is the reference for the S/H "Hold" pulse in Gating and No Timing modes of operation. The Internal Trigger Circuit derives a trigger pulse from the zero crossing of the epBPM input signals.

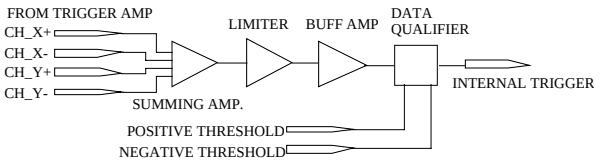

Figure 5. Internal Trigger Circuit

The Summing Amplifier (gain 1/2 - one channel) (Fig. 5) output signal is the sum of the signals from four trigger amplifiers (Fig. 2). Its output feeds the Limiter input. The limiter amplifier output signal range is limited to ±1V. This increases the dynamic range of the internal trigger circuit. Limiter output goes through the Buffering Amplifier (gain 2) to the Data Qualifier. The Data Qualifier consists of two threshold comparators and one zero crossing comparator. The thresholds levels determine

the level of the lowest signal which could be "seen" by the Data Qualifier. Potentiometers are used to adjust threshold level. The Data Qualifier generates a single trigger pulse synchronous with zero crossing event, 30 ns duration time. After generation of one pulse the Data Qualifier is ready for the next zero crossing event.

5. TIMING CIRCUIT AND CAMAC INTERFACE

CAMAC instruction decoding, timing distribution and data conversion are performed in a Field-Programmable Gate Array (FPGA). The following blocks are programmed in the FPGA: CAMAC instruction decoding; power startup (to load calibrated delay data); Calibrator control - to send CAL_GO pulse, to set attenuators values and to select pulse polarity; ADC control - to read data from the ADC, to reset the S/H driving circuit; Pedestal Trigger control - to start pedestal calibration; Trigger Modes control- to select trigger mode; Delay control - to load data to delay DL_1 - DL_6. Data and timing signal are distributed over the epBPM module via 8-bits local bus or individual traces. A crystal oscillator, 30 MHz ferquency, is used as reference for the internal clock.

6. MODULE SPECIFICATION AND BENCH TESTS RESULTS

The estimations of the epBPM module resolution and dynamic range are based on accurate calculations of the circuit noise level. The ADC signal-to-noise plus distortion ratio (SINAD) is 78 dB using a 50kHz input signal, 300 kHz sampling rate. The effective number of bits (N_{eff}) from the SINAD:

$$N_{eff} = \frac{SINAD - 1.76}{6.02} \approx 12.7$$

So the quantization error σ is:

$$\sigma = \frac{q}{\sqrt{12}} \cdot 2^{(N_{id} - N_{eff})} \approx 0.7 \cdot q,$$

where q is the ADC quanta's size, N_{id} - ideal ADC number of bits. Thus $\sigma \approx 610$ μV, or 434 μV rms. The OA3 (Fig. 2) input noise in 4 MHz bandwidth is 22 μV rms, the S/H noise is specified as 65 μV rms, OA1 input noise in 100Mhz bandwidth is 25 μV rms. Total noise value at the input of OA1, including 14 μV rms noise, generated by resistors, is 54 μV rms or 15.4 dB, refered to 50 Ohms resistance noise value in 100 MHz band. The signal processing channel gain is 10, so the equivalent ADC input noise is 540 μV rms [2].

The dynamic range is 6.5×10^3 or 76 dB (the ratio between the ADC maximum input signal and circuit noise at the ADC input). Resolution (Δx) is [3]:

$$\Delta x = \frac{a}{2\sqrt{2}} \cdot \frac{V_N}{V_0},$$

where V_N - is the rms noise value at the OA1 input, V_0 - is the bunch peak voltage for the beam in the center, a - is the half of beam pipe aperture (9 mm).

The measured bunch peak voltage from the Linac stipline electrode, connected in series with the S/C and Filter is 200 mV at 3.8×10^{10} particles per bunch (ppb) for the beam in the center. For this number of particles per bunch the resolution is ≈0.9 μm. The required resolution, specified at 5×10^{10} ppb is the 5 μm, the calculation gives 0.7 μm. The calculated resolution for PEPII 5×10^8 ppb (minimum) is 65 μm and for 10^{11} ppb (maximum)it is 0.5 μm.

Bench tests give less than 3.5 μm resolution of the beam position with the Calibrator pulse, corresponding to 1.52×10^{10} ppb. This is worse than the 2 μm estimated for this value, but better than 16 μm, derived from the required 5 μm. The resolution limiting factor is the difference of the propagation delay between peak and zero crossing for electron and positron- like pulses in the Internal Trigger circuit. The result is - different programmable delays values for the pulses with different polarity of the first peak. To achieve the best resolution for both pulses, an average delay value is used.

The measured dynamic range in the External Trigger mode with external pulser is 68 dB (pulser dynamic range), in the Internal Trigger it is 48 dB. In the Internal Trigger and Gated mode dynamic range is limited by noise, coming from the digital part of the epBPM board and from external sources.

7. SUMMARY

The Two-Bunch Beam Position Monitor design and specifications have been discussed. The bench tests results have been described. Comissioning of the epBPM modules has been planned for May, 1997, so the tests results may be available at conference time.

8. ACKNOWLEDGEMENTS

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[3] "Beam Position Monitoring", Robert E. Shafer, AIP conference proceedings 212, Accelerator Instrumentation, Upton, NY 1989