DEVELOPEMENT OF A DIGITAL LONGITUDINAL DAMPER FOR THE TLS STORAGE RING

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Abstract

A digital longitudinal damper is being developed in SRRC to stabilize the longitudinal coupled-bunch instabilities observed in the TLS storage ring. It is a bunch by bunch feedback system designed for 200 bunches at 2 ns bunch interval. Designs of the bunch phase detection circuit, the digital electronics and the 1125 MHz wideband rf system for correction of phase errors are presented in this article. The core of the digital electronics is a DSP array that ultilizes commercially available DSP modules performing parallel processing at a data throughput of 500 Mbytes/sec. This will greatly reduce the time required for both hardware and software developments. A prototype operating at one eighth of the data rate of the final system is under construction to evaluate the system design.

1 INTRODUCTION

Longitudinal coupled-bunch instabilities (LCBI) ocurred in the TLS storage ring electron beam are driven by cavity high order modes (HOMs) [1]. Since the bunch current is below the microwave instabilities threshold, LCBI is the main obstacle in preserving low emittance at higher beam current. Further, sudden amplitude changes of such instabilities are undesirable to the users because photon flux through slits fluctuate significantly [2]. In order to reduce the amplitude fluctuation of the instabilities, the original HOM damping antenna on each of the two cavities was replaced by an auxilliary tuner for detuning the troublesome HOMs [3]. Improvement of photon beam stability by an order of magnitude is achievable. However, the amplitudes of the LCBI are still significant. An active longitudinal damper is indispensable to suppress the instabilities effectively.

The damping system and some major subsystems designs will be described in section 2. The status of the project will be discussed in section 3.

2 SYSTEM DESIGN

The damping system being developed is a DSP based bunch by bunch feedback system. That is, the phase of each bunch is individually locked to the master clock signals [4]. For a system manipulating hundreds or thousands of bunches, a feedback system based on digital signal processing tecniques takes the advantage of simplicity in hardware structure in comparison with the mode by mode feedback. Also, the flexibility of such system allows conductions of various tasks with the same hardware design. For example, the longitudinal feedback system can be used to analyze the dynamics of the longitudinal dipole motions of the bunched electron beam.

The design of this longitudinal damper is conceptually similar to the ALS or PEPII system. In order to reduce the system development time and considering the ease of software development and maintenance, we employ very well developed commercial DSP modules that support real time parallel signal processing. Also, efforts have been made to simplify the interface between A/D (D/A) converter and the DSP modules. This interface circuit has the functions of down sampling, demultiplexing, multiplexing and data I/O control of the DSP modules. As shown in Figure 1, front end of the system is a phase detection circuit operating at 6 times of the rf frequency. The phase errors are digitized by an 8 bits flash A/D conveter at 500 Ms/sec and the data are then down sampled and distribute to the individual chips in the DSP array by the demutiplexer and a controlled FIFO memories. The array consists of eight DSP modules, each module has four DSP chips that perform digital filtering (e.g. FIR filters) such that the phase error information of the bunches can be extracted. The processed data are reorganized in a proper sequence again by the controlled FIFO memories and the multiplexer. The digital signal in this sequence is convertered back into a single analog signal by a fast D/A converter. This analog signal modulates the 1125 MHz rf system that is used to drive the feedback cavity. It is a low Q cavity providing a fast changing kick voltage to the beam. System design parameters are listed in Table 1.

Table 1. Parameters of the TLS Longitudinal Damper

rf frequency	500 MHz
bunch interval	2 ns
bunch numbers	200
synchrotron tune	0.0115
beam pickup frequency	3000 MHz
phase detection range	±15° max.
kicker frequency (bandwidth)	1125 MHz (250 MHz)
maximum kicker strength	200 volts
down sampling factor	16
number of filter taps	5
numbers of DSPs	32

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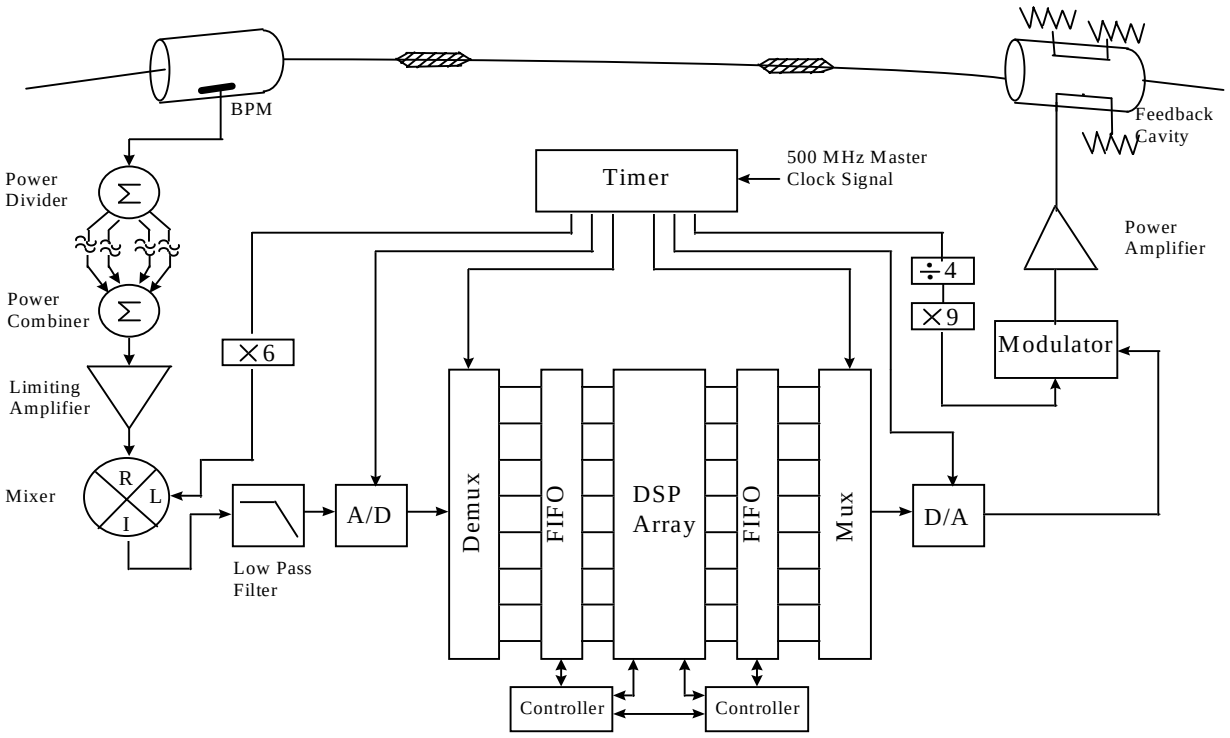

Figure 1. Functional Diagram of the TLS Longitudinal Damper

2.1 Bunch Phase Detection

Bunch signal picked up from a BPM electrode is used to generate short burst so that the phase error can be detected by common mixer techniques (see Figure 1). Since the bunch interval is 2 nsec. and the phase detector is designed to operate at 3 GHz, the dynamic range of detector is limited to ± 15° of the rf signal. Duration of the burst is limited to 1.4 nsec so that the detected phase error of one bunch can not be interferred by the signals of the neighboring bunches. This 3 GHz burst train is generated by a pair of four way broadband power dividers (combiners) connected by four short coaxial cables. The length of each cable is adjusted to have a group delay of 333 psec longer than the next cable. The phases of the short bursts relative to a 3 GHz reference signal are measured by a double balanced mixer. The 3 GHz reference signal is an Elisra MW15700 active multiplier which multiplies the 500 MHz master by six times and therefore phase locked to the clock signal. The IF output from the mixer are filtered by a 250 MHz low pass for anti-aliasing.

2.2 The wideband RF System

The rf system used to correct the phase errors of the bunches is designed to operate at 1125 MHz. The 1125 MHz signal to the power amplifier is locked to the rf frequency. It is generated by dividing the rf frequency four times and multiplied nine times (by another Elisra MW15700 active multiplier). In order to provide at less 250 MHz bandwidth for phase modulation, the 200 Watts Hughes instrumentation TWTA that have instantaneous bandwidth from 1 to 2 GHz is employed. The design of the modulator is not finalized yet. Since the modulation bandwidth of an I & Q modulator is inherently wide, the possibilty of using such network as phase modulator is under study.

The longitudinal kicker is essentially a pill-box cavity in TM_{010} mode except that it is heavily damped by coupling rf power out with large area magnetic coupled loops external rf absorbers. One of the coupling loop is used to couple the power output from the TWTA into the feedback cavity. Numbers of N-type rf coaxial feedthroughs are used to separate vacuum from the atmosphere. The advantages of using external loads are: (1) one can adjust the gain and bandwidth of the system by simply changing the loading condition of the cavity even it is in vacuum. (2) power combination can be made simply by connecting a TWTA to another coupling loop. From the cold tests we have done for a prototype kicker, a loaded Q of 4 can be obtained. The theoretical shunt impedance is approximately 100 Ω.

A vacuum compactable high power version that made of stainless steel with embedded cooling channel is currently under construction. Other issues that may affect the kicker performance such as beam loading, beam induced voltages etc. are under study in detail.

2.3 Digital Signal Processing

The core of the longitudinal damper is the DSP array. In our design, it consists of eight VME DSP modules. Each module can have four TMS320C40 40 MHz floating point parallel DSP as the processing elements. Since the chip have six 20 Mbytes/sec bidirectional communication ports, it allows communications between processors or direct data I/O controlled with external circuits. We use the 4 chips DBV44 DSP boards produced by Loughborough Sound Images as an example. It has eight uncommitted communication ports available via the front panel that can be used as the direct data I/O to the processors. On-board JTAG implementation enables cluster of C40 DSPs to be debugged in parallel. Software support such as the C source debugger, C compiler and the DSP function library are considered as the advantages of using such modules. Since floating point calculation is not necessary in our usage, it is considered to be a drawback of using C40 as the processing elements because it needs two extra cylcles to conveter the 8 bits fixed point data to floating point data and convert them back.

The A/D conveter we used is the MAX101 8 bits flash A/D converter that operates at 500 Ms/sec. It has dual 250 MHz outputs that are 180° out of phase. One of the main task is to make down sampling and distribute the data to the DSP array in a proper order. This is done by the demultiplexer and the controlled FIFO (first-in first-out) memories. The FIFO controller is programmed by PLD (Programmable Logic Devices). An overview of the digital signal processing electronics is shown in Figure 3.

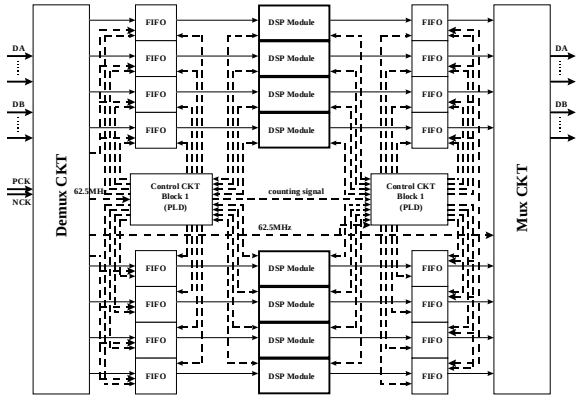

Figure 3. An Overview of the Digital Signal Processing Electronics.

Figure 4 shows demultiplexer circuit done by the serial to parallel converter MC100E445. A multiplexer for processed data reorganization is just the reverse of the demutiplexer logic. The fast D/A converter generates the analog modulation that is used to correct the beam. The TQS TQ6122 8 bits, 1 Gs/s digital-to-analog converter will be used for this purpose.

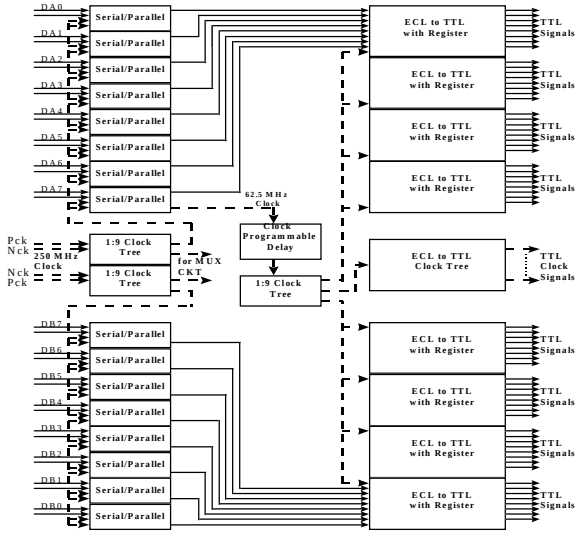

Figure 4. Functional Drawing of the Demultiplexer

3 STATUS OF THE PROJECT AND THE PROTOTYPE SYSTEM

A prototype system is being built to demonstrate the validity of the design as discussed in the previous section. Since we use one DSP board (with PCI bus and installed on a PC), this system can only operate at 62.5 MHz that is one eighth of the full speed of the final system. It can handle 25 equally spaced bunches. The MAX101 fast A/D converter circuit board has been built, tested and performs correctly. Since the designs of the D/A converter and the modulator are not finalized yet. We will use the Merrimac JEM-2B 1125B QPSK modulator that can be driven directly by the ECL signal in the multiplexer of this prototype system. This QPSK has a norminal data rate of 50 Mbits/s but still works fine at 62.5 Mbits/s.

The final system is scheduled to start commissioning by the end of this year.

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