ARC DETECTION AND INTERLOCK MODULE FOR THE PEP-II LOW LEVEL RF SYSTEM*

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Abstract

A new arc detection and interlock generating module for the SLAC PEP-II low-level RF VXI-based system has been developed. The system is required to turn off the RF drive and high voltage power supply in the event of arcing in the cavity windows, klystron window, or circulator. Infrared photodiodes receive arc signals through radiation resistant optical fibers. Gain and bandwidth are selectable for each channel to allow tailoring response. The module also responds to interlock requests from other modules in the VXI system and communicates with the programmable logic controller (PLC) responsible for much of the low-level RF system's interlock functionality.

1 SPECIFICATION AND DESCRIPTION

The PEP-II low-level RF system VXI-based Fast Interlock module (figure 1) performs several functions related to monitoring and protecting the RF system. The module serves as the sole VXI module responsible for transmitting any VXI module generated faults to trip the klystron high voltage system. Each Fast Interlock module resides in a VXI crate adjacent to each RF station. An additional hardware subsystem known as the 'Local Panel' has been configured to serve as an intermediary between the interlock handling subsystems of the VXI Fast Interlock module, the Allen-Bradley (Milwaukee, WI) PLC, and the high voltage power supply (HVPS) controller[1].

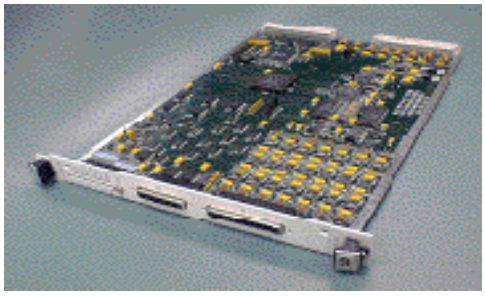

Figure 1. VXI Fast Interlock Module

The Fast Interlock module communicates directly with the Local Panel and indirectly through it to the Allen-Bradley system and the high voltage power supply controller.

Fiber optic cables monitor for high power arcing near the cavity windows and at the klystron and circulator.

2 I/O FACILITIES

The Fast Interlock module provides a means of communicating with several external systems. The control system can operate the HVPS, klystron filament and solenoid supplies, and beam abort requests as well as Allen-Bradley system monitoring and fault resetting. The ethernet fiber signals from the control system are brought into the shielded rack and passed on to the Fast Interlock module by a National Instruments (Austin, TX) VXIcpu-030. The Fast Interlock module then issues the commands over fiber optic cable to the nearby instrumentation rack containing the Local Panel.

In the event of a fault it can be necessary to abort the beam to prevent instabilities from the undriven RF cavities. A global beam abort system receives the request to abort the beam from the Fast Interlock module and the request is maintained until either the cavities of that station are parked or the station is returned to normal operation.

An uncommitted external input for tripping of the system is available.

3 ALLEN-BRADLEY COMMUNICATIONS

The RF system is monitored by an Allen-Bradley PLC/5 industrial controller. This Allen-Bradley controller monitors numerous temperatures, digital inputs, and analog voltages. If any of the monitored levels goes outside its prescribed range a fault signal is sent to the Fast Interlock module which then turns off the high voltage. The controller also sends a 'heartbeat' signal over a fiber optic cable to the Fast Interlock module. Should this pulse train fail to appear at the Fast Interlock module after a suitable time, the Fast Interlock module will assume the controller is faulty and issue a command to turn off the high voltage.

The processing nature of the Allen-Bradley system precludes its use as a fast interlock generator. The system loops through its monitored signals approximately once every 15 ms. This is adequate to respond to 'slow' problems, like faulty temperatures, arising in the RF system, but is not adequate as a means of tripping the

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system in the fast manner required such as when an arc is detected.

A separate chassis serves to collect the many fiber optic connectors, both inputs and outputs. Each arc detection fiber input connects here. The fiber connections for the control of the filament supply, HVPS, solenoid, Allen-Bradley reset, Allen-Bradley heartbeat, Allen-Bradley summary, and beam abort signal are on this chassis. The optical signals are converted to electrical signals and transmitted over ribbon cable to the Fast Interlock module nearby.

4 COLLECTOR POWER DETECTION

The klystron forward power is detected in the external chassis and an analog output sent to the Allen-Bradley system for use in tripping the system if the collector power is too high. This is determined by subtracting the klystron forward power from the high voltage supply's voltage-current product and assuming that the difference is absorbed in the collector.

5 INTERLOCK HANDLING

All critical fast interlock logic resides in hardware on the Fast Interlock module. The fault logic is independent of the crate controller microprocessor and network. Should there be a network problem or crate controller hang-up the Fast Interlock module will still function to trip the HVPS in case of a fault. All faults are configured in a fail safe manner so as to trip the system in event of module failure. The fiber optic outputs must provide continuous light output in order for the 'on' signal to be valid. Power loss to the module leads to the turning off of the high voltage. The primary interlock function is through the permissive for the HVPS that is issued from the Fast Interlock module. Other modules in the crate may be configured to issue interlock requests to the Fast Interlock module by asserting a TTL backplane trigger. These faults may be generated for reasons of excessive RF amplitude detected on any number of monitored signals such as klystron reflected power.

The high voltage permissive is removed by the Fast Interlock module when any of the fault sources is in the faulted state. The VXI backplane trigger, the loss of the Allen-Bradley heartbeat or summary, a detected arc, or even a software generated forced fault may all drive the fault line. A 'first fault' register is provided in the event of a rapid succession of faults in order to distinguish the precipitating fault. The current status as well as latched fault status is available to read out in the event that a fault is persistent. A front panel trigger is provided when a fault is detected for additional diagnostic purposes.

The VXI backplane fault requires special handling by the Fast Interlock module since it is a fault that is both generated by and monitored by the module. Upon detecting any type of fault the Fast Interlock module asserts the backplane TTL trigger for the benefit of the other modules. In the event another module in the crate is forcing the fault the Fast Interlock module must remove its assertion and check for persistent assertion by the other module and maintain the fault if that assertion is there.

6 ARC DETECTION

Seven 100 foot lengths of fiber optic cable bring the arc detection light to the Fast Interlock module. In a high energy ring installation four are from cavities, one is from the klystron window, and another is from the circulator, the seventh is a spare channel. A low energy ring installation has two fewer cavities to monitor. The detector is a Honeywell HFD-3854 PIN photodiode with a peak response wavelength of 850 nm. Each channel has both adjustable gain and bandwidth setting jumpers. The fastest response time is about 1μs. The slowest can be up to 10μs. Slower settings enable controlled timing of the trip. The circulator manufacturer specifies a 5μs trip time to allow for burning up the arc instigating debris. Three gain settings along with adjustable trip settings at the comparator input allow flexible selection of trip levels for good protection without nuisance trips. The photodiode output is amplified in two stages to achieve a gain of about 155dB. The two feedback stages are implemented in a 'T' topology (figure 2) to allow moderate component values and reduced stray capacitance.

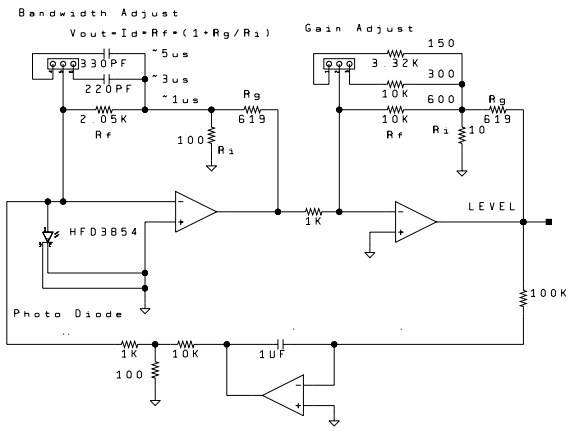

Figure 2. Photodiode Preamp Schematic

Each channel has slow DC removal (>1ms) to allow the use of high gain without regard to the offsets that would normally restrict such a gain. Only fast transient light

events are triggered. The unbiased response time of the photodiode is fast enough that no reverse biasing is required. The resulting speed increase from reverse biasing would be small compared to overall response time anyway, and dark current noise would increase. The noise equivalent power is approximately .05μW (-43dBm). The preamp output is buffered and available at the front panel of the external chassis for testing and monitoring purposes.

The two-stage output is then transmitted differentially to the VXI module portion of the fast interlock system. Each of the channels may be bypassed through a jumper located on the VXI module itself. Remote readback of the bypassed status is provided.

The fiber optic cable for the arc detection is Spectran (Avon, CT) HCR with 200 micron core. The cable is UL rated OFNP -- Nonconductive Optical Fiber plenum cable, no conduit is required and it meets safety standards for flammability and smoke generation. The cable is radiation resistant and should be able to reside in the PEP-II tunnel without degradation. The cable has been tested elsewhere with up to 50 krads without degradation[2]. Radiation dose in the PEP-II beam tunnel where the fiber resides is estimated to be approximately 30krad/year [3]. The only component of the Fast Interlock system to reside in the beam tunnel is the radiation hardened fiber optic cable. Less than one third of the length of each cable resides in the tunnel radiation area. Test data shows approximately 1dB induced loss per 30m of exposed cable after a brief exposure to 3krads [4]. Fiber optic cable of this type is known to recover over a period of time subsequent to the dose. This provides assurance that the arc detection system will not be significantly 'blinded' by beam loss events.

7 CRATE TEMPERATURE AND VOLTAGE MONITORING

A programmable data acquisition system (DAS) monitors the crate temperature and power supply voltages and generates an interrupt in the event of an out of tolerance value. Once programmed, the DAS reads through its channels comparing the inputs to programmed limits without control system attention.

The peak detected levels from the arc detection channels are available through the control system to assist in remote trip level setting and noise monitoring.

8 CONCLUSION

A VXI-bus based Fast Interlock module is in use in the PEP-II low-level RF system. It is required to handle numerous sources of faults and transmit trip requests rapidly and reliably. The crucial interlock logic resides entirely in hardware and operates autonomously despite computer or network difficulties.

9 REFERENCES

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