EVALUATION OF IEEE 1394 SERIAL BUS FOR DISTRIBUTED DATA ACQUISITION*

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Abstract

One trend in accelerator instrumentation is the digitization of signals further upstream in the signal processing chain. In some systems, this leads to distributed data sources that must be interconnected in a standard way. IEEE 1394 Serial Bus provides a possible interconnection standard for these systems. With Serial Bus, data acquisition is implemented via memory to memory transfers within a distributed 64 bit address space. Because this functionality is provided in silicon, software overhead is significantly reduced. This technology is under evaluation for use in the RHIC position monitor system. Using this example system, the suitability of IEEE 1394 for the accelerator environment will be described. Also, the results from recent tests will be presented.

I. INTRODUCTION

Before the introduction of card modular packaging like CAMAC and VXI, electronic instrumentation was typically housed in separate chassis and interconnected with cables. Modular systems introduced standard packaging that allowed inter-module communication via a well defined parallel backplane. Additional benefits include compactness and the convenience of a shared power supply. Although this packaging works for most accelerator instrumentation systems, some applications could benefit from the old separated chassis solution. Examples include: systems with large components that make inefficient use of circuit board real estate, distributed systems that must consolidate data from digitizers located close to the signal sources, and high performance devices that must operate in a controlled environment. After the decision is made to remove devices from the backplane environment, the requirement for data communication remains.

In this brief paper we cannot compare the many communication standards that could connect separate chassis. Of the many standards available, the IEEE1394 Serial Bus[1] offers a reasonable trade-off between cost, performance, and distance. Also, the standard is based on a memory mapped model that allows simple bridging to existing VME/VXI systems. Silicon support and industry acceptance is growing. The RHIC beam instrumentation group is evaluating IEEE1394 for use in the position monitor system.

II. OVERVIEW OF IEEE1394 SERIAL BUS

Some of the most important Serial Bus features are listed below:

- Memory mapped model based on the IEEE 1212 Command and Status Register (CSR) standard with a 64 bit addresses.
- 100, 200, or 400 Mbits/s bandwidth. Work is in committee to extend the standard to 3.2 Gbit/s.
- Hot pluggable and self-configuring.
- Asynchronous (guaranteed delivery) and isochronous (guaranteed bandwidth and latency) data transfers are supported.
- Up to 4.5 meters between nodes, 72 meter total length. Work is in progress to extend to much longer distances.
- Cable or backplane environments. The cable environment is specifically designed for low emission and susceptibility.
- Point-to-point signal transmission. Each node re-clocks data before re-transmission.
- Cost effective: Silicon cost $30USD/node in 1997.

The memory mapped model makes the protocol fairly efficient. In fact, memory to memory transfers between nodes can be supported in silicon with no software overhead. However, latency is only guaranteed at the 125 μs level. To maintain efficient media use, split transactions are supported. When bridging Serial Bus to a backplane bus that does not support split transactions (like VME), some decoupling must be provided to avoid backplane bus time-outs.

Although this standard was developed for short haul communications in consumer-oriented multimedia systems, it has potential for longer distance operation and for industrial applications. A 1394 system with 100 meter hops over plastic optical fiber has been demonstrated as part of the home network initiative[2]. The noise immunity and isolation provided by this solution would be welcome in the accelerator environment. One of the earliest deployments of 1394 in an industrial application is an electrical power network simulator developed by Sederta for

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HydroQuebec[3]. Installed at Mitsubishi in Kobe, Japan in July 1996, the first system consists of 8 SUN workstations with two 1394 interfaces each, 75 VME based PowerPC CPU nodes with two 1394 interfaces each, and 120 I/O nodes each containing 4 Industry Pack sites and one 1394 interface.

III. RHIC POSITION MONITOR APPLICATION

The RHIC position monitor system includes over 600 channels (planes) of electronics, each housed in their own chassis. Because there are only six major equipment buildings external to the tunnel, most channels will be located in the tunnel, adjacent to their corresponding position monitor. This arrangement improves performance and tremendously reduces cable cost. Where the position monitors are located near the equipment buildings or in high radiation areas, signals will be cabled out of the tunnel on pairs of high quality, phased matched coax. The electronics chassis will be identical for all channels. The distributed chassis will be mounted above the magnet cryostats while the others will be rack mounted.

Each channel contains two 16 bit samplers operating at a nominal rate of 78 kSamples/s (the revolution frequency of RHIC). An onboard DSP provides buffer maintenance, digital filtering, local control, and built in self test features. Data communication between the position monitor modules and the VME based control system will be provided by approximately four independent IEEE1394 buses per VME system. Each bus will contain about 12 nodes with each node separated by up to 20 meters. Achieving reliable communication over these distances in an accelerator's EMI environment is the early goal of our evaluation program.

Each distributed channel will continuously update a circular buffer with averaged beam position records. These records are typically calculated at a rate of about 100Hz. The buffer will be located in VME-resident memory that is bridged to a portion of the Serial Bus' 64 bit address space. In addition, a subset of channels may be selected to stream turn-by-turn position samples into VME memory. To allow efficient use of bus bandwidth, the Serial Bus asynchronous block transfer capability will be used. Although isochronous transfers would provide the most efficient bus utilization, guaranteed delivery is more important at this low level of the data acquisition chain. Therefore, the system will allow a retransmission of corrupted packets (as identified by the built in 32 bit CRC circuitry). This capability is only available to asynchronous transfers because they include an acknowledgment packet for every transfer.

Two 1394 mezzanine cards have been designed and constructed for this application. The first, an Industry Pack supporting the 100Mbit/s rate has been used to exercise basic 1394 functionality and to demonstrate packet transmission over a 20 meter long cable. The second, a PCI Mezzanine Card (PMC) is a candidate for use in the final system and will be used in a 12 node demonstration system by late 1997.

IV. THE 1394 INDUSTRY PACK

The Industry Pack 1394 module (IP1394) is a double wide Industry Pack[4] that uses the first generation Texas Instruments 1394 chip set, namely the TSB12C01A link layer controller and the TSB11C01 physical layer controller. A block diagram of the IP1394 is shown in Figure 1.

This module was constructed in 1995 and primarily used as a stepping stone to the final module, the PMC1394, which will be described later in this paper. The Industry Pack Interface Bus permitted us to use an existing VME-based carrier board, which contains a DSP96002[5]. The DSP96002 assembles/disassembles packets to/from the 1394 bus and provides bridging between 1394 and VME address spaces.

The TSB12C0l link layer controller provides all necessary control and status registers, as well as three FIFOs for sending and receiving packets. To transmit a packet, quadlets are written to the Asynchronous Transmit FIFO, or the Isochronous Transmit FIFO, depending on the type of transaction required. These FIFOs are written one quadlet at a time until the complete packet is in the FIFO. The TSB12C01A then requests the bus through the TSB11C01. The TSB11C01 arbitrates for the bus and upon successful arbitration forwards the packet from the TSB12C01 onto the 1394 bus. Incoming packets are received by the TSB11C01, retransmitted out its other two ports, and forwarded to the TSB12C01 if the bus and node number are a match. To read the incoming packets, the General Receive FIFO on the TSB12C01 is read, one quadlet at a time until the entire packet is received.

The major limitation of the IP1394 is its lack of galvanic isolation between the Link Layer Controller and Physical Layer Controller. This creates ground loop problems when attempting to use multiple IP1394

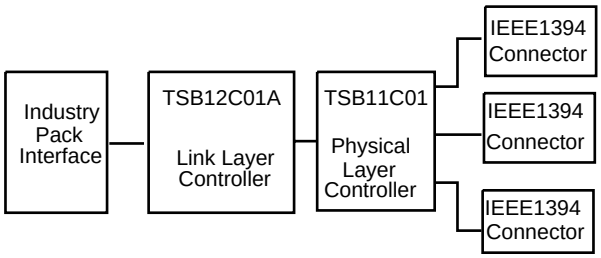

Figure 1. Block Diagram of IP1394

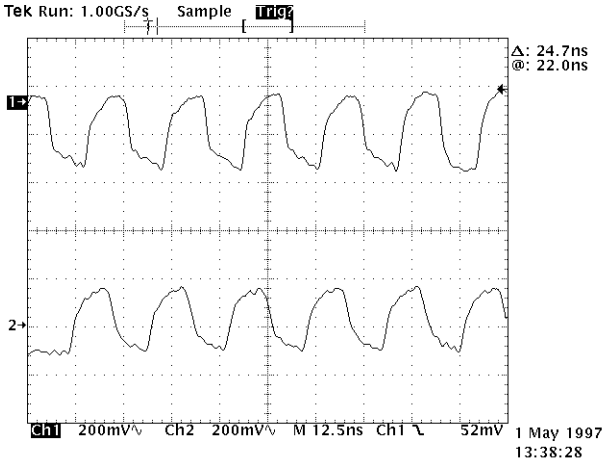

Figure 2. 100 Mbit/s data over 20m cable (top: input, bottom: output)

modules powered from different supplies. This problem has been addressed in the PMC1394 module.

Figure 2 shows a sample waveform of the 1394 strobe line transmitted by the IP1394 for a single data quadlet packet over a 20 meter cable. The cable was specifically designed by C&M Corporation for 1394 transmissions up to the 200Mbit/s rate. Signal fidelity at 100 Mbit/s is good enough to expect adequate reliability.

V. THE 1394 PMC BOARD

The 1394 PMC[6] board (PMC1394) uses the Texas Instruments TSB12LV21 (PCILynx) and TSB21LV03 (PCIPhysical) chip set with the isolation feature implemented. The PCILynx IC provides a high performance IEEE1394 interface with the capability to transfer data between the 1394 physical link interface, the PMC bus interface and external devices connected to the local bus interface. It contains the link layer controller (LLC) which is the control for transmitting and receiving 1394 packet data between the FIFO and physical layer IC at 100, 200 or 400 Mbps and allows access to the physical IC control and status registers. The PMC interface supports 32 bit burst transfers up to 33 Mhz. The PCILynx IC also includes a DMA controller with 5 DMA channels, as well as a local bus interface consisting of RAM, ROM, AUX, ZV (video), and GPIO (general purpose I/O). Only RAM and GPIO are implemented on the PMC1394 board. There are 4 GPIO ports with status monitoring LEDS and 32K x 16 bits of RAM. The board includes a 2K serial eeprom allowing the loading of configuration registers and unique identification codes.

The IEEE1394 cable carries data at various rates and also sources/sinks power to/from remote nodes. This allows nodes that either do not have their own source of power or have their power turned off to continue to function as repeaters in the IEEE1394 network. The PMC1394 board conforms to the requirements set forth

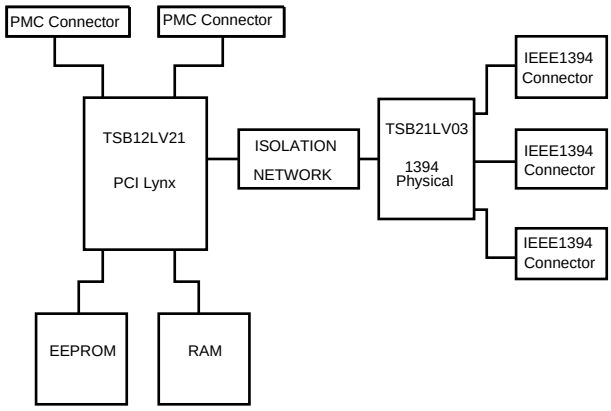

Figure 3. Block diagram of the PMC1394

in the IEEE1394-1995 specifications for isolation concerning shield termination, cable power isolation and signal isolation. The board achieves signal isolation by using the method known as a bus holder galvanic isolation barrier. It consists of a series isolation capacitor between each of the PCILynx and PCI Physical IC's signal lines with CMOS bus holders on each side of the capacitor. Control lines are isolated by using opto-isolators. Power isolation is handled by a DC-DC converter for 1394 cable power. The cable shield is isolated per the specification by connecting the outer cable shield to ground through a parallel combination of a 1 M ohm resistor and a 0.1 microfarad capacitor to provide a relatively high impedance coupling at low frequencies and a relatively low impedance coupling at high frequencies.

VI. FUTURE WORK

A demonstration system consisting of 12 nodes with a hop length of up to 20 meters will provide confirmation of a reliable operation. This demonstration in a high EMI environment will be required before procurement of the RHIC position monitor electronics. Performance optimization will then commence.

VII. REFERENCES

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