THE RHIC REAL TIME DATA LINK SYSTEM*

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Abstract

The RHIC Real Time Data Link (RTDL) System distributes to all locations around the RHIC ring machine parameters of general interest to accelerator systems and users. The system, along with supporting host interface, is centrally located. The RTDL System is comprised of two module types: the Encoder Module (V105) and the Input Module (V106). There is only one V105 module, but many (up to 128) Input Modules. Multiple buffered outputs are provided for use locally or for retransmission to other RHIC equipment locations. Machine parameters are generated from the V115 Waveform Generator Module (WFG) or from machine hardware and coupled directly through a fiber optic serial link to one of the V106 input channels.

1 BACKGROUND

Many magnet excitation currents will be related to the beam energy or similarly to the main magnet dipole current. To avoid manual adjustment of hundreds of excitation currents to track the main magnet dipole current, the RTDL System provides for the distribution of real time data on the main magnet dipole current and other machine parameters in a form that can be used directly by equipment control hardware.

2 INTRODUCTION

The RTDL machine parameter frames are transmitted on a serial self clocking link using a modified Manchester code (bi-phase mark). Each frame has the following format:

* 1 start bit
* 8 bit parameter ID field
* 24 bit parameter Data field
* 1 parity bit
* 1 stop bits

The transmission rate is 10Mb/s and 3.5μs are required to transmit each parameter data frame. All frames are transmitted synchronous with the 720 Hz RHIC Event (every 1.39 ms). The 8 bit parameter ID field allows up to 255 different frames to be defined, and sufficient time exists for transmission of all 255. The system transmits a continuous bi-phase mark "one" (the 10Mhz carrier) during idle periods. This scheme of transmission is the same as the Event Link currently being used in the AGS/Booster Timing System, and therefore can take advantage of existing fanout and repeater circuits.

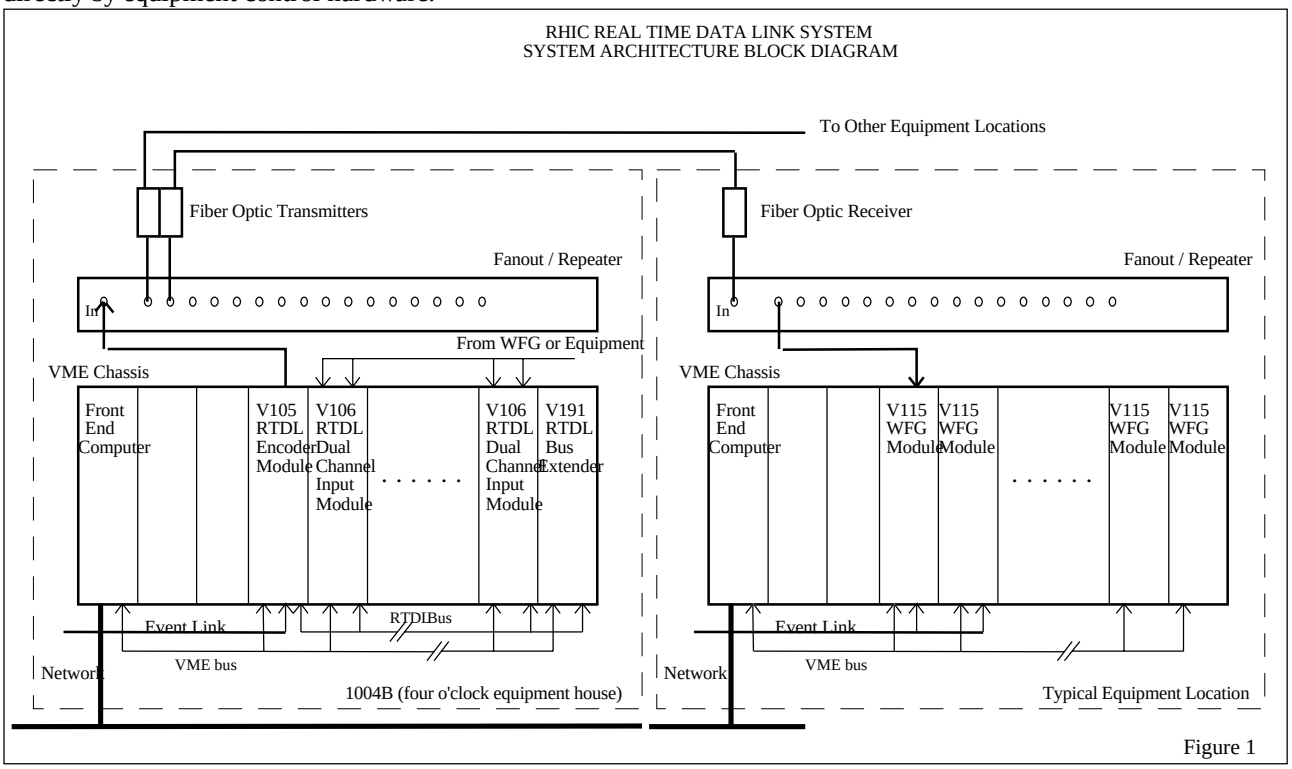

Figure 1

* Work performed under the auspices of the U.S. Dept. of Energy.

3 SYSTEM ARCHITECTURE

The RHIC RTDL System is located in the 4 o'clock equipment house (1004B). A standard 6U 84HP VME Chassis has sufficient space to support the V105 module, the necessary V106 modules to support 30 RTDL frames, the standard Front End Computer (FEC) running VxWorks operating system used in all RHIC VME chassis, and a V108 utility module. Additional frames can be added with extension chassis. The V105 initially drives a fanout/repeater module which provides multiple buffered TTL differential outputs. These outputs are used locally within the 4 o'clock equipment house, and others drive fiber optic transmitters for optical transmission to other RHIC equipment locations. Local receiving modules are isolated from the V105 module by transformer coupling at the receiving modules input.

At each equipment location, the optical transmission is converted to single-ended TTL, and buffered as differential TTL. A fanout/repeater is utilized to generate multiple outputs. General purpose V108 Utility modules which receive the RTDL frames may be located in these area, as well as specially designed modules such as the V115 WFG, which have direct RTDL inputs. A block diagram of the overall system architecture is shown in figure 1, and the front panel layout for each module is shown in figure 2.

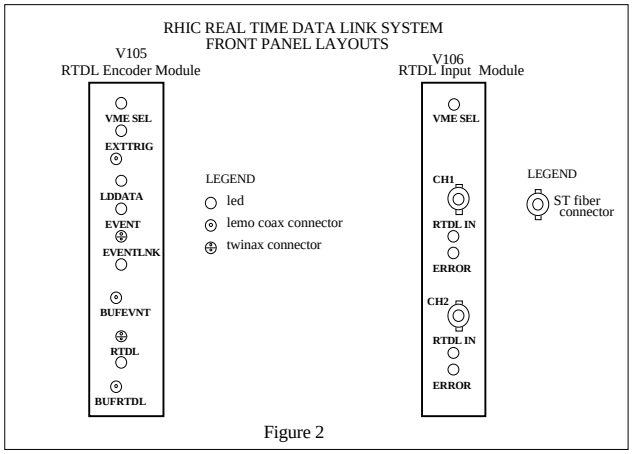

Figure 2

A hardware block diagram for the V105 and V106 modules is provided in figure 3. The V105 Module contains a VME bus interface, RHIC event link interface, the custom interface (local) bus control circuitry, the parameter ID SRAM and the link encoder circuitry. The V106 module contains a VME bus interface, the direct machine parameter input interface and a custom interface (local) to the V105 module through user defined pins on the VME bus P2 connector.

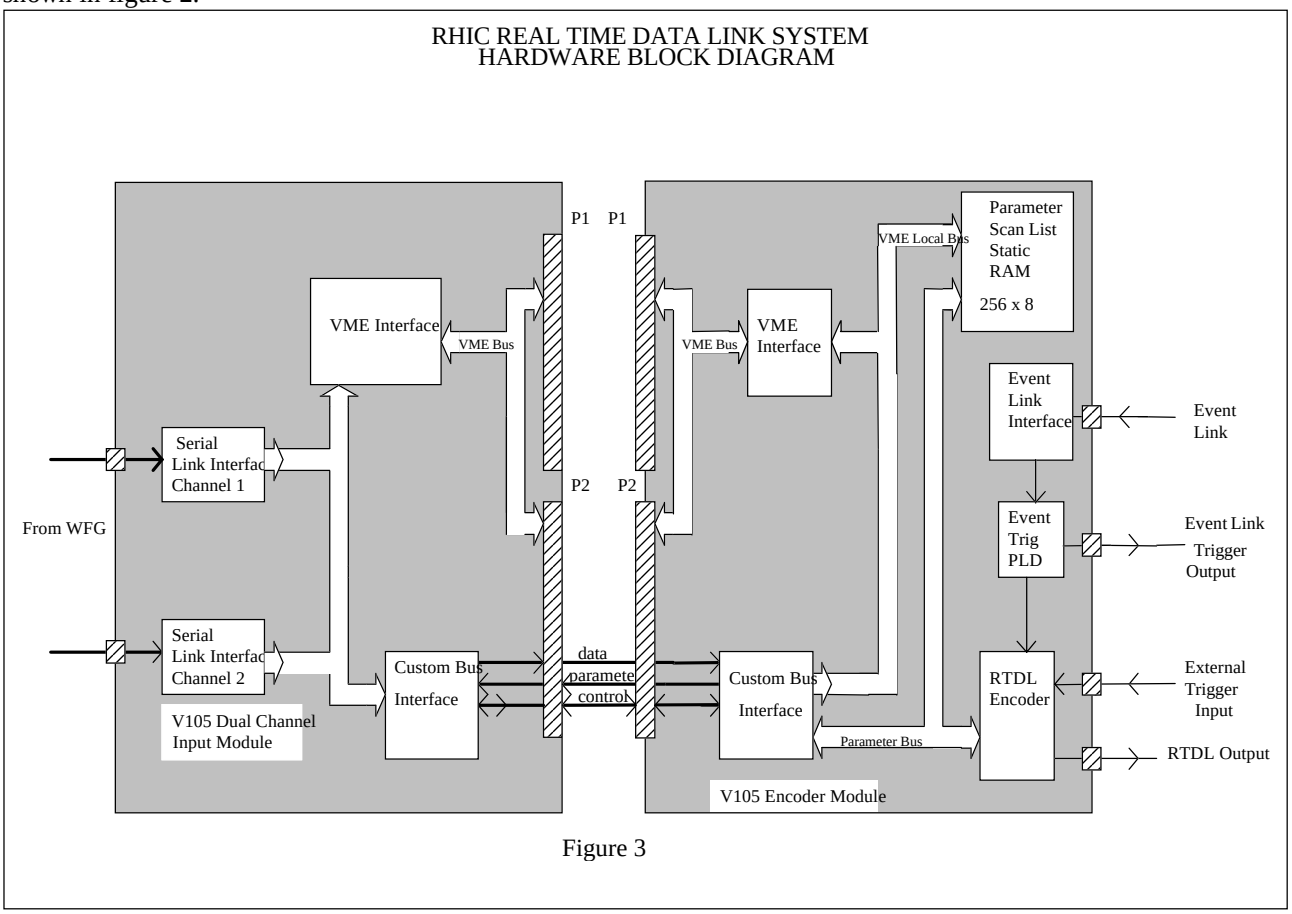

Figure 3

4 THEORY OF OPERATION

4.1 V105 Encoder Module

The V105 Module is a standard VMEbus 6U x 160mm module. It occupies 4HP of a standard 84HP VME chassis. This module directly outputs the encoded machine parameters onto the link. It accepts parameter data from the V106 modules via the custom interface bus. The V105 module controls the handshaking protocol on this bus.

The V105 Module converts each machine parameter acquired from the V106 from a serial NRZ into a serial bi-phase mark code for transmission. Parameter frames are permanenetly assigned a parameter ID code. Parameter transmission priority is defined in the parameter ID SRAM. The V105 module contains a RHIC Event Link interface which decodes the 720 Hz event, and initiates a transmission cycle synchronous with this event. For RTDL System diagnostic purposes, an external user supplied trigger or a RHIC Event Link trigger (other than the 720 Hz event) can initiate a transmission cycle. There is no system limitation that frames be transmitted in sequential order.

When the transmission cycle has been triggered, the following will occur:

a. A parameter ID code, which was previously defined in the SRAM, will be made available on the custom interface bus for all V106 modules to read.
b. The channel whose parameter ID matches the one placed on the bus, places its' machine parameter data on the custom interface bus.
c. Data is latched into the encoder modules' output register.
d. The RTDL encoder is triggered and the data is encoded and transmitted as one frame.
e. This process continues until all defined frames have been transmitted. The "end of list" is defined as 00h.

If any channel has not responded within 1μs, an interrupt will
be generated, and the parameter ID of the nonresponsive channel will be stored in the status register.

The V105 Module is a VMEbus slave. Status/ID registers (64 bytes), scan list RAM (256 bytes), and configuration registers are mapped to VME A16 space on a jumper selectable 512 byte boundary (A16..A9). VME data transfers supported include D16 and D08(EO), except for the scan list RAM, which allows D08(EO) only. BLT (block mode transfer) is not supported.

4.2 V106 Input Module

The V106 Module is a standard VMEbus 6U x 160mm module. It occupies 4HP of a standard 84 HP VME chassis. Each module has two input channels. Parameter data to be transmitted on the link can be input from one of two sources:

a. various system sources on unique serial fiber optic links .
b. written to the individual channel via the VMEbus interface.

Separate registers are provided on each input channel for storing both the machine parameter data and VME supplied data. A command to each channel input selects the source of the data to be transmitted on the link. A strobe, synchronous with the 720 Hz event, transfers the content of the selected source register for each input channel to its respective output register. The content of both the machine parameter data register and the VME register can be read through the VMEbus interface. The parameter ID for each input channel is jumper selectable on the input module, and can be read via the status register.

When the V105 module initiates a transmission cycle and places a parameter ID on the custom interface bus, the following will occur:

a. All input channels will decode the parameter ID.
b. The channel that matches the code placed on the bus places the contents of its output data register on the custom interface bus and completes the data transfer by asserting a data acknowledge strobe.
c. Custom interface bus cycles continue until all channels have been polled.

The V106 Module is a VMEbus slave. Status/ID registers (64 bytes) and configuration registers are mapped to VME A16 space on a jumper selectable 256 byte boundary (A16..A8). VME data transfers supported include D16 and D08(EO). BLT (block mode transfer) is not supported.

5 REFERENCES

[1] Ducar, R. J. , *CAMAC 166 Module - MDAT Transimitter*, Fermi National Lab Controls Hardware Release No. 45.3, 8/25/88.

[2] Hartmann, H. , *Specification for the RHIC Real Time Data Link System* , 10/23/93, unpublished.