A BUNCH CLOCK FOR THE ADVANCED PHOTON SOURCE

Frank R. Lenkszus and Robert J. Laird
Advanced Photon Source, Argonne National Laboratory
9700 South Cass Avenue, Argonne, Illinois 60439 USA

Abstract

A bunch clock timing module has been developed for use by Advanced Photon Source beamlines. The module provides bunch pattern and timing information that can be used to trigger beamline data collection equipment. The module is fully integrated into the control system software (EPICS) which automatically loads it with the storage ring fill pattern at injection time. Fast timing outputs (1 ns FWHM) for each stored bunch are generated using the storage ring low-level rf and revolution clock as input references. Fiber-optic-based transmitters and receivers are used to transmit a 352-MHz low-level rf reference to distributed bunch clock modules The bunch clock module is a single-width VME module and may be installed in a VME crate located near beamline instrumentation. A prototype has been in use on the SRI CAT beamline for over a year. The design and integration into the control system timing software along with measured performance results are presented.

1 INTRODUCTION

The need arose to provide bunch timing for a time-resolved experiment at the APS. The primary requirements were to provide a timing trigger for each bunch stored in the machine and to provide a means for adjusting the timing of the bunch triggers to compensate for propagation delays.

We considered both a centralized bunch clock generator with individual time delays for multiple beamlines and distributed bunch clock generators. The module described in this paper may be used either way. We presently plan to provide a separate module for each beamline, i.e., distributed bunch clocks. The reasons are twofold: it is much easier to distribute a clean, stable rf reference than a train of impulses, and separate bunch clock generators allow the tailoring of trigger sequences to individual experimental requirements.

2 DESCRIPTION

The bunch clock accepts both the storage ring revolution clock and 352-MHz low-level rf as inputs. It provides two NIM-level outputs that have a sequence of pulses corresponding to bunches stored in the ring. The output pulses are synchronized to the low-level rf input and hence are synchronized to the beam. Each output bunch pulse is approximately 1 ns wide.

Coarse and fine programmable delays are provided to adjust the output timing to the arrival of beam at the experimental apparatus. The coarse delay is specified in low-level rf tics and is variable from 0 to 1295 (the ring has 1296 rf buckets). The fine delay has a range of 0 to 4.6 ns with a resolution of approximately 18 ps per step. The combination of the two delays permit the output to be shifted up to a full revolution period with 18 ps resolution.

The module also provides a raw bunch clock output. When used with multiple programmable external delays, the output provides the basis for a centralized bunch clock generator.

3 CIRCUIT

The bunch clock circuit is shown in Fig. 1. It is based on an arbitrary bit pattern generator. The contents of an on-board RAM is shifted out a bit at a time at the storage ring rf frequency. Each bit in the RAM corresponds to a storage ring rf bucket The shifting process is synchronized with the revolution clock such that the bit sequence starts over at each revolution clock. The RAM is loaded with the bunch pattern at injection time.

Two inputs are required: the revolution clock and the low-level rf reference. The revolution clock is resynchronized with the rf reference. The resynchronized revolution clock is delayed by a counter which produces an output delayed by a programmable number of rf clock periods. This counter provides the coarse delay. The delayed revolution clock resets a divide-by-16 counter that advances the RAM address counter. The 16 data outputs of the 256-word RAM are loaded into a shift register which runs at the rf reference rate. The output of the shift register is fed to a programmable digital delay chip which controls the fine delay with a resolution of approximately 18 ps per step.

The delayed shift register output is buffered through NIM output buffers that drive the front panel bunch clock output connectors. In addition, the shift register output is buffered and brought out as the “raw bunch clock” signal. This signal may be used with external circuits to provide additional outputs.

It takes 81 16-bit RAM memory locations to hold the 1296-bit storage ring bucket pattern. The RAM address counter is compared to the value “81” and reset when that value is reached.

It is absolutely necessary that the revolution clock arrive at the front panel within an acceptable time window relative to the rf reference input to assure stable operation. A timing circuit compares the received revolution clock arrival time with the rf reference. A status indicator available as a front panel LED indicates whether or not the timing is acceptable. The revolution clock may be shifted one-half an rf period by a two-position front panel “skew” switch.

0-7803-4376-X/98/$10.00 © 1998 IEEE

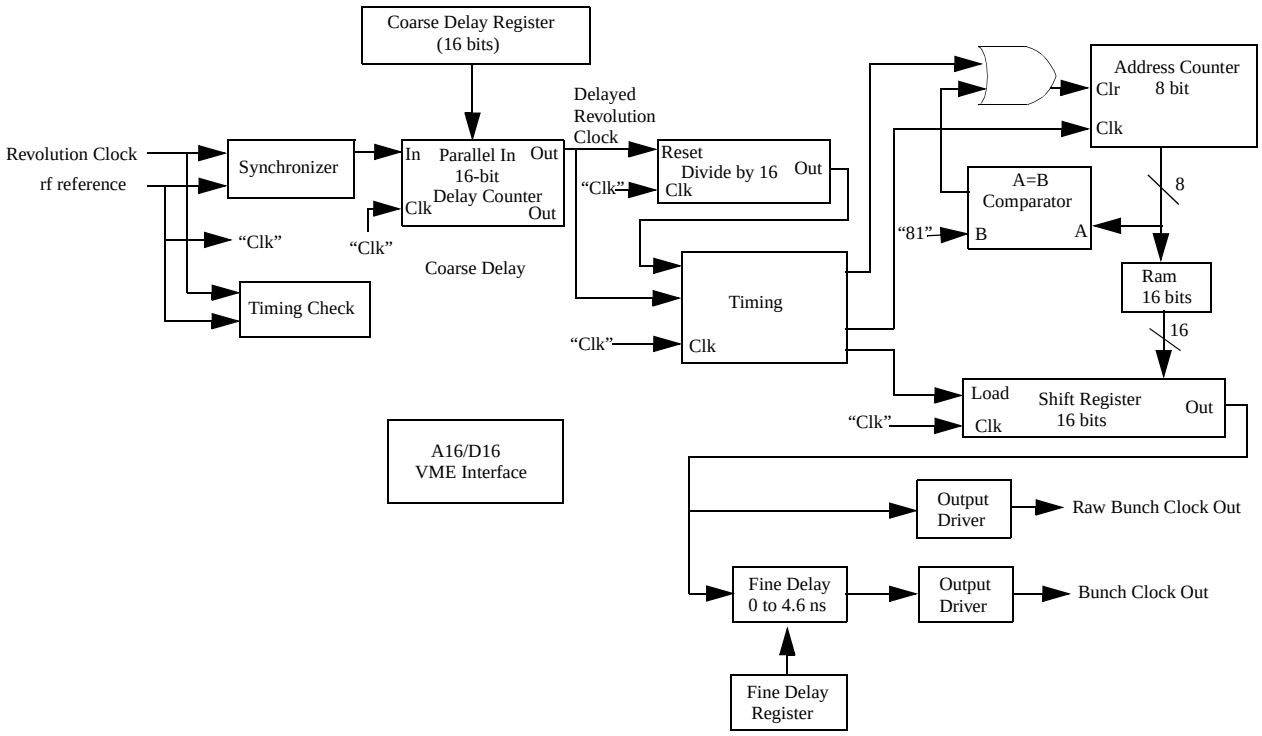

Figure 1: Storage ring bunch clock block diagram.

Since the revolution clock is used only to reset the divide-by-16 counter that advances the RAM address counter, the circuit has the interesting property that it will continue to produce a synchronized bunch pattern output even if the revolution clock is momentarily lost. This is neither the normal nor desired mode of operation. This property, however, illustrates the choice of a design that provides a modicum of fault tolerance.

A VME interface provides read/write access to the bunch pattern RAM and to registers that set the coarse and fine delays. Status readbacks are provided that indicate whether or not the rf reference and revolution clock inputs are receiving signals.

4 IMPLEMENTATION

Most of the circuit is implemented with emitter-coupled logic (ECL). The VME interface and RAM addressing logic are implemented in PLDs. The edge speed of ECL, 125 to 300 ns, dictates the use of controlled impedance lines on the printed circuit board. As a result, the circuit was implemented on an 8-layer board. In addition, the fast edge speed requires that printed circuit line stub lengths be held to a minimum.

The logic is fully synchronous. A great deal of care has been taken in distributing the clock and minimizing clock skew. Differential clock drivers with guaranteed within-device clock skew of less than 50 ps are used to provide clocks to various parts of the circuit. In addition, printed circuit board trace lengths have been adjusted to minimize skew at critical parts of the circuit. As part of a test of internal timing margins, we are able to run the bunch clock generator reliably at 480 MHz. In fact, the bunch clock generator may actually be capable of running in excess of 500 MHz. The 480-MHz limit is imposed by a module that generates the revolution clock. If the revolution clock input is removed, the bunch clock will run at a rate in excess of 550 MHz.

The circuit is implemented in a single-width VME card. An on-board DC-to-DC convertor provides the -5.2 Volts required by the ECL logic.

5 SOFTWARE

Software has been written to seamlessly integrate the bunch clock generator into the APS control system. An EPICS device driver, database, and graphical control screens have been developed which provide access to all the bunch clock generator features.

The bunch clock generator programming model is straightforward and consists of five registers. The registers are control/status, RAM address, RAM data, fine delay, and coarse delay. The EPICS driver provides a convenient interface to these registers through EPICS process variables.

EPICS process variables are provided to enable/disable the bunch clock output, clear the bunch pattern RAM, set and reset a bit in RAM corresponding to a desired bucket number, return a waveform listing the filled bucket numbers, and return a waveform showing the bunch pattern as an array of ones and zeros.

The set and reset process variables accept a bucket number as the input value. The driver computes the RAM location and bit number corresponding to the desired bucket number and sets or resets the resultant bit in the computed RAM location.

The storage ring injection timing system writes the value of each bucket number to the bunch clock set bucket number process variable as part of the storage ring injection process. Thus, the bunch clock generator RAM contents track the injected bunch sequence as bunches are injected into the storage ring.

The bunch clock generator RAM contents need to be cleared upon loss of beam. An EPICS state program implements the logic to perform this function. The state program monitors storage ring beam current. When the beam current drops below a setable threshold for more than 5 seconds, the bunch clock clear bunch pattern process variable is written, causing the device driver to clear the RAM contents.

In addition, upon causing the bunch pattern waveform record or the filled bucket numbers waveform records to be "processed" (an EPICS euphemism for causing a database record to perform its intended function), the device driver reads the RAM contents and computes and returns either bucket numbers or the bunch pattern depending on which process variable is processed.

6 RF REFERENCE DISTRIBUTION

Since the bunch clock generator is intended to be located near the beamline, an important consideration in the design is delivering the rf reference to the bunch clock generator front panel. While a coax cable such as phase-stabilized HELIAX® may be used (and in fact this is exactly what we used initially), we designed a pair of single-mode fiber optic modules to deliver the rf reference to distributed bunch clocks from a central location.

7 PERFORMANCE

Tables 1 and 2 summarize measured performance. Temperature measurements were done in an environmental chamber at 23 +/- 10 degrees C.

The measured value of 34 ps/degree C/km should be compared to an estimated 19 ps/degree C/km for HELIAX® LDF2-50.

Table 1: Temperature Measurements

	ps/degree C
Fiber transmitter	7
Fiber receiver	0
Single mode fiber	34/km
Bunch clock	10 (estimated)

All jitter measurements were made with a 20-GHz sampling oscilloscope. The quoted rms jitter is as calculated by the oscilloscope. Peak-to-peak jitter was measured by placing the oscilloscope in infinite persistence and measuring the peak-to-peak spread over a two-minute period.

Table 2: Jitter Measurements

	rms	peak to peak
Bunch clock	3.4 ps	21 ps
Fiber transmitter - 525m fiber cable - fiber receiver	3.2 ps	25 ps
In situ at Sector 3	5.3 ps	36 ps

The end-to-end measurement for the fiber transmitter and receiver for a short (2 m) cable resulted in essentially the same values as reported for the 525-m fiber length.

The in situ measurement was done at the SRI CAT. The cable run to this location is approximately 115 m. A HELIAX® cable with 352 MHz driven from the same location as the fiber was used as a reference. We believe this overestimates the jitter somewhat.

8 CONCLUSIONS

The bunch clock generator was placed in production in January 1996. It has been successfully used for several time-resolved experiments at SRI CAT. A second bunch clock is scheduled to be installed at the BESSRC CAT in May of this year. It is anticipated additional units will be installed as more beamlines move into production.

9 ACKNOWLEDGMENTS

Work is supported by the U.S. Department of Energy, Office of Basic Energy Sciences, under Contract No. W-31-109-ENG-38