DIGITAL LOW LEVEL RF SYSTEMS FOR FERMILAB MAIN RING AND TEVATRON

B.E. Chase, B. Barnes, K. Meisner, Fermilab†, P.O. Box 500, Batavia, IL 60510

Abstract

New Low Level RF systems are successfully operating the Fermilab Main Ring and Tevatron. The upgrade replaces aging CAMAC and NIM components, and increases system accuracy, reliability, and flexibility. VXI LLRF systems feature a custom three channel direct digital synthesizer (DDS) module capable of independent or ganged operation in both frequency and phase modulation. Frequency and phase values are computed at 100Khz by the module's Analog Devices ADSP21062 (SHARC) digital signal processor. The DSP concurrently handles feedforward, feedback, and beam manipulations. Higher level state machines and the control system interface are handled at the crate level using the VxWorks operating system. This paper discusses the hardware, software, and operational aspects of these LLRF systems.

1 SYSTEM HISTORY

CAMAC and NIM (CNIM) platform LLRF systems have served Fermilab accelerators well for many years. The new Main Injector and Recycler accelerators, future Tevatron 36 on 36 collider HEP, and increasingly complex operating scenarios and study programs require significant and correspondingly complex new LLRF system functionality. Many future LLRF requirements are difficult to implement in the CNIM platform.

CNIM LLRF systems are very hardware intensive, with a large number of distributed specialty modules and cabling complexity for parallel digital data, timing, and DC through RF analog signals. Frequent upgrades introduce hardware changes and new EMI issues, and often require adding hardware in limited physical space.

Limited CNIM processing power means important LLRF feedforward control programs are manually tuned tables written to CAMAC curve generators. They do not incorporate fundamental accelerator physics and are not responsive to actual accelerator parameters. More complex control algorithms like the Main Ring LLRF synchronous phase angle program are accomplished by a combination of curve tables and electronic "tricks". This can produce errors that exceed the operating range of feedback loop components, and means scenarios like Main Ring (and future Main Injector) deceleration become unduly elaborate and esoteric implementations.

Future beam transfers between the Main Injector and Tevatron (transfer cogging) and collision point control in the Tevatron (collision point cogging) argue for replacing the CNIM cogging LLRF system, [*1] if only because simultaneous CNIM support of both cogging processes is difficult and very hardware intensive.

CNIM LLRF state machines execute in many modules. Minor system upgrades involve significant state machine hardware re-engineering, plus rematching RF amplitudes, group delays, and phase offsets. It is effectively impossible to duplicate and test CNIM system operation in a lab environment.

2 VXI SYSTEM COMPONENTS

The VXI platform facilitates LLRF system development and improves performance by shifting implementation into powerful hardware and software. The systems consist of modules in a single VXI mainframe and a custom interface chassis. About a dozen cables provide the control system network connection, accelerator time and data, TTL I/O, and LLRF outputs.

The front ends are National Instruments cpu-030 VXIbus embedded computers running VxWorks. The VXIcpu-030 is configured for slot 0 operation and runs a Startup Resource Manager with strict interpretation of the VXIbus specification to verify and configure all system devices. NIcpu-030 code libraries and an ethernet port provide all communication with control system host computers through the usual ACNET protocol. All cpu-030 software is downloaded over the network.

Fermilab VME and VXI Universal Clock Decoder (UCD) modules receive and process Tevatron clock (TCLK), Beam Synch clock, and MDAT [*2] accelerator timing and data. The UCDs synchronize LLRF system processes and provide ACNET interface timing resources.

An Interface Technologies IO100VXI digital I/O module generates TTL signals to other systems. It drives local comfort displays on a custom interface chassis that also filters and distributes the system RF outputs.

A Fermilab Direct Digital Synthesizer (DDS) with a SHARC DSP generates three LLRF outputs, and is a key component discussed in following sections. All VXI DDS modules receive a 50Mhz LO signal and 25Mhz DSP clock from a single ovenized crystal Oscillator module. The OSC module also sources the VXI backplane CLK10 signal. DSP software is downloaded over the network through the cpu-030.

A two channel 200Khz 16bit ADC module connects directly to the DDS via the local bus DSP serial port.

A lab VXI development system exactly duplicates operational systems and is used extensively to verify functionality before installation in the accelerators.

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† Operated by Universities Research Association Inc. under contract with the U.S. Department of Energy

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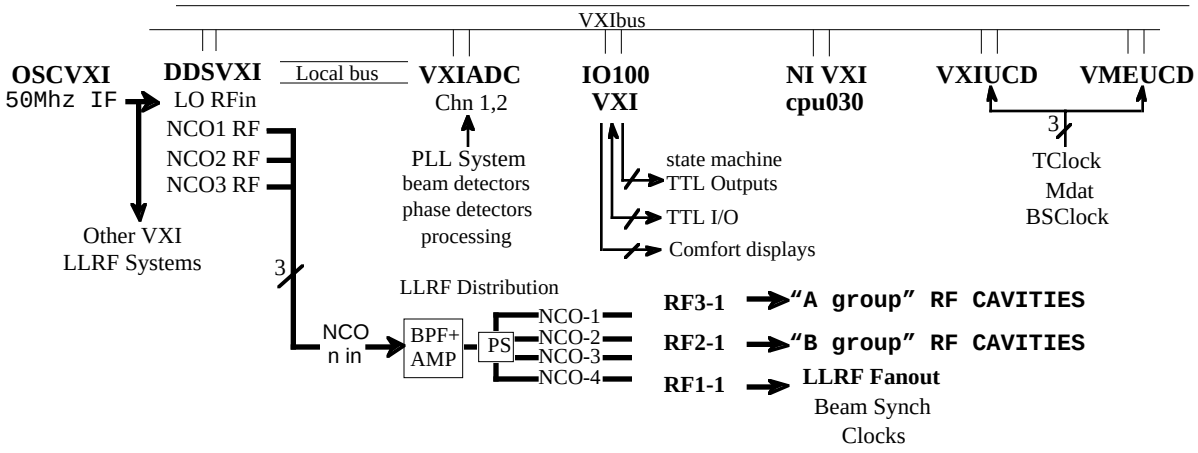
VXI LLRF Block Diagram



3 DDS HARDWARE

The VXI Direct Digital Synthesizer (DDS) is a custom module designed to provide LLRF frequency and phase control. It has three RF synthesizer channels controlled by an Analog Devices ADSP21062 (SHARC) DSP. Frequency and phase control for the RF channels can be independent or ganged. The DDS is a VXI slave with full interrupt and VXI trigger capability. High speed serial and link port DMA data paths are provided over the VXI local bus for real time feedback.

Each synthesizer channel consists of a Numeric Controlled Oscillator (NCO), two DACs, and an IQ modulator. The NCO is a Harris HSP45106 with 32 bit center frequency and 16 bit phase control registers which provide milli-Hertz and 100 micro-radian resolution. NCO outputs are 16 bit sine and cosine values. The TTL sine and cosine values drive separate 12 bit DACs. The nominal 3MHz DAC outputs are filtered to remove alias spectra, and drive the I and Q ports of the Mini-Circuits MIQC-88M modulator. The 50MHz OSC module drives the modulator LO port, and clocks the NCOs at 25MHz. The modulator RF output is the upper sideband 53MHz signal that is amplified to +17 dBm and output to the DDS front panel. A coupled port is provided for monitoring.

This configuration provides the following benefits. The lower sideband, LO leakage and IF harmonics are spaced at 3MHz intervals from the 53MHz RF drive. These signals are greater than -40dBc and are easily filtered outside the DDS module. Close in spurs are small due to the low distortion and quantization noise of the 12 bit DACs. Phase noise is near the extremely low level of the crystal oscillator. Phase control accuracy is very precise, as any nonlinearities in the IF path produce harmonics which are again attenuated by the bandpass filter. Synchronism between the NCOs on frequency register writes is essential for maintaining coherent phase. A virtual NCO (NCOALL) is decoded by hardware to generate common register write and control strobes.

PLL output signals are presently digitized with the two channel ADC module. ADC serial data is transferred over the VXI backplane local bus to DSP memory by the SHARCs DMA controller. Data can also be transferred from a 4 channel 12bit 25Mhz ADC module over the backplane using the SHARC local bus. These transfers are also under DMA control, and can run at 25Mbytes/sec.

4 DDS SOFTWARE

The DSP and its software create the RF bucket while controlling bucket area, beam energy, and azimuthal positions. It must do this as gently and with as little RF phase noise as possible to avoid heating the beam. This requires that DSP code execution is very deterministic, frequency and phase calculations are smooth and accurate, and that sidebands created in the process are small and outside the RF cavity bandwidth.

The feedforward frequency program (Frf) is calculated from real time bend bus current broadcast at 720Hz.

$$F_{rf} = F_E\big|_{(\Delta r=0)} = F_\infty \beta = F_\infty \left(1 + \frac{K}{I^2}\right)^{\frac{-1}{2}}$$

where $F_\infty = \dfrac{hc}{2\pi R_0}$

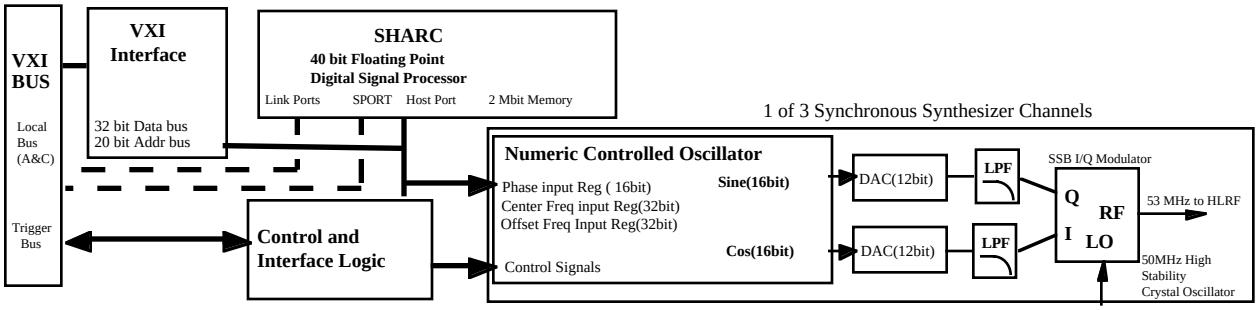
The DSP interpolates Frf at 100KHz with a 7.5Hz lowpass 2760 tap FIR filter. Frequency feedback is also applied at 100Khz. The synchronous phase angle is calculated from I dot and the RF cavity gradient Vg.

$$\phi_s(t) = \sin^{-1}\left(\frac{2\pi R_s}{ecV_g\beta_s}\frac{dE_s}{dt}\right)$$

DDS phase control provides many LLRF system beam control processes. There are seven phase control input categories grouped by function and bandwidth requirements. 720hz adiabatic inputs are: static OFFSETs for transfer phasing, group delay COMPENSATION, Φs CALCULATIONs, SLOW arbitrary WAVEFORMs for counterphasing, and bucket COGging waveforms. Non-adiabatic 16.6Khz inputs are: STEPs for transition jumps

and FAST arbitrary WAVEFORMs. The DSP applies all categories simultaneously and several categories have multiple inputs. All DDS phase control data is interpolated and output at 100Khz. Lock stepping of the three process rates is done by a scheduler that is phase locked to the 720Hz MDAT link with a software PLL.

Asynchronous DSP processes such as cogging or transition crossing are driven by hardware and software interrupts. Priorities for these interrupts are set lower than the 720hz/16.6Khz/100Khz synchronous processes. The cpu-030 host communicates with the SHARC via its message and vector interrupt (VIRPT) registers. The model follows a C call in that DSP input parameters are written to message registers, and the interrupt is generated when a DSP function pointer is written to the VIRPT. DSP return and error values are placed back in the message registers. All DSP code is a continuation of the object models formed in the cpu-030 libraries.



5 VXI SYSTEM OPERATION

Finite state machine implementation in front end and DSP software is a key VXI LLRF system feature that has demonstrated many advantages. The system VXIUCD sources backplane interrupts and triggers from directly decoded TCLK events and events + delays. These high priority LLRF system events are state machine excitations connected to corresponding callback functions. Users describe system operation in common accelerator language on a dedicated console application program. The user requests are sent to the front end with normal Acnet protocol to condition state machine outputs. State machines can also use VXIUCD MDAT 720hz accelerator data as conditional inputs.

One category of conditional inputs is used to completely reconfigure LLRF state machines for any specific accelerator cycle, and every cycle can support all functionality. Fermilab LLRF systems constantly evolve to support new operating scenarios and study programs that must be completely parasitic to normal operation. The state machine configuration inputs and the lab development system have proven invaluable for verifying new system functionality.

State machine outputs are largely IO100VXI digital I/O module TTL signals, and VIRPT calls to the DDS module. A state machine logging feature provides state execution timing, output values, and messages that offer intelligent problem diagnostic capability. Automatic test suites for component verification and run time fault detection are incorporated with no additional hardware.

6 SUMMARY

The VXI platform's accurate real time control has improved LLRF system performance. The DDS Frf calculation has decreased the MRLLRF frequency error from ±12Khz to ±350hz. This allowed a corresponding reduction of the beam PLL gain and CLBW, and reduced phase noise in the MRRF system. Accurate Frf has been exploited by state machine options that run the DDS open loop at specific frequencies. This feature is used anywhere the magnet current is constant, to eliminate transfer PLLs and replace CNIM flattop oscillators and RF switches.

The accurate DSP synchronous phase angle calculation eliminated MRLLRF problems from limited range feedback loop components, and allowed MR beam deceleration back through transition for the first time.

The VXI platform has streamlined LLRF systems by replacing dozens of CNIM modules and hundreds of cables. Adding basic accelerator physics to deterministic and responsive processors has improved performance, increased functionality, and minimized tuning. Concentrating LLRF state machines into easily managed code libraries has facilitated performance upgrades. Basic state machine control for parasitic MR slip stacking studies was added in hours. Transfer and collision point cogging were decoupled by adding cogging support to the VXI MRLLRF and TVLLRF systems in an upgrade that required no hardware modifications.

ACKNOWLEDGMENTS

The LLRF Group thanks Charlie Briegel for help with the ACNET interface, and Keith Engell for work on the LLRF console application.

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