DESCRIPTION AND OPERATION OF THE LEDA BEAM-POSITION / INTENSITY MEASUREMENT MODULE*

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Abstract

This paper describes the specification, design and preliminary operation of the beam-position/intensity measurement module being built for the Low Energy Demonstration Accelerator (LEDA) and Accelerator Production of Tritium (APT) projects at Los Alamos National Laboratory. The module, based on the VXI footprint, is divided into three sections: first, the analog front-end which consists of logarithmic amplifiers, anti-alias filters, and digitizers; second, the digital-to-analog section for monitoring signals on the front panel; and third, the DSP, error correction, and VXI-interface section. Beam position is calculated based on the log-ratio transfer function.. The module has four, 2-MHz, IF inputs suitable for two-axis position measurements. It has outputs in both digital and analog format for x- and y-position and beam intensity. Real-time error-correction is performed on the four input signals after they are digitized and before calculating the beam position to compensate for drift, offsets, gain non-linearities, and other systematic errors. This paper also describes how the on-line error-correction is implemented digitally and algorithmically.

1 INTRODUCTION

This paper describes the specification, design and preliminary operation of the beam-position/intensity measurement module for the LEDA and APT projects at Los Alamos National Laboratory. It is one sub-system of the entire beam-position measurement system described more fully in references [1] and [2]. Related parts of the system include the down-converter module and the error-correction reference chassis. A block diagram of the position/intensity measurement module is shown in Fig. 1. The measurement technique is based on the log-ratio transfer function which has been described by several authors [3,4,5]. The log-ratio technique is defined as

$$V_{\log ratio} = \log(T) - \log(B) \qquad (2)$$

where T and B represent the intermediate-frequency signals for opposite top and bottom lobes of a beam-line probe. Subtraction is easier to perform than division and can be done either by digital or analog techniques.

The module is divided into three sections: first, the analog front-end; second, the digital-to-analog section; and third, the DSP, error-correction, and VXI-interface section. Some of the important specifications of this module are listed in Table 1.

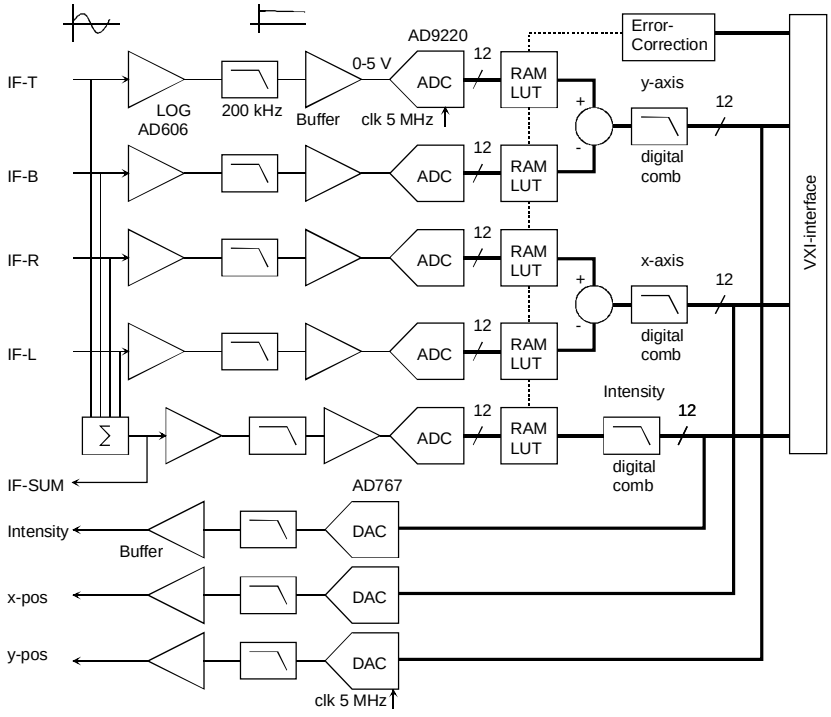

Fig. 1 Block diagram of the position/intensity module.

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Table 1. Requirements for the LEDA/APT Beam Position/Intensity Module.

Item	Value	Units
Frequency input (IF input)	2.00	MHz
Maximum input signal power	15	dBm
Input impedance	50	Ω
# of IF inputs	4	each
# of axis measurements/module	2	each
Range, x-, y-axis outputs	±10	V
Range, intensity output	0-10	V
Measurement bandwidth	≥ 180	kHz
Measurement resolution	0.03	dB
ADC Resolution	12	bits
ADC sampling rate	5	MHz

2 ANALOG FRONT-END

Referring to Fig. 1, the analog section is comprised of the AD606 log amplifiers, the 200-kHz anti-alias filters, the IF summer, and the ADCs. The log amplifiers are rated to 50 MHz with usable dynamic range in excess of 80 dB [6]. A typical curve for the AD606 is shown in Fig. 2. The data were taken from -80 dBm to +20 dBm. There is some distortion at the

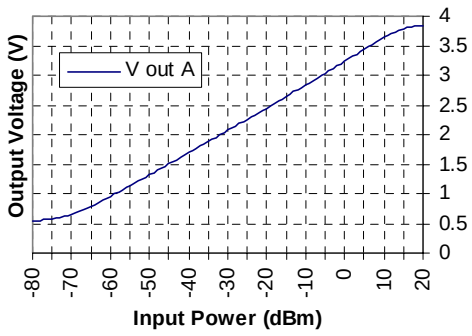

Fig. 2 Vout vs. input power for a typcial AD606 log amp operating at 2 MHz.

upper end starting at an input power of about 15 dBm due to saturation and also at the lower end of the input range where the log amp approaches the reference level. The ideal response for this log amp is

$$V_{out} = K \log\left(\frac{v_{in}}{v_{ref}}\right) \quad (3)$$

where v_{in} is the rms amplitude of the input signal , v_{ref} is 8.60 μVrms (corresponding to -88.3 dBm reference level), and K=0.75 [7]. Since the log amp is non-ideal, there are small perturbations in its transfer function and distortion effects at the upper and lower ends of the dynamic range. By using digital error-correction, non-ideal performance in the log amps and other system non-linearities can be taken out of the overall transfer function of the system.

The output of each log amp is filtered with a 200-kHz anti-alias low-pass filter. After the low-pass filters, each signal is over sampled at 5 MHz by an AD9220 12-bit ADC. The signal-level range at the input of the ADCs is 0-5 V. The voltage resolution using 12 bits and 5 V is ±0.61 mV which corresponds to a probe dB offset resolution of ±0.0163 dB. The resolution in mm depends on the specific probe sensitivity.

The four IF-inputs are combined in the IF-SUM circuit to be used to measure beam intensity by a fifth log amp channel. This IF-SUM signal is also available to other accelerator systems via the module's front panel. Even though the sum of the four signals is a non-linear response to beam intensity if the beam is off center, knowing beam position in x-and y-space, and measured intensity, the real beam intensity can be calculated. This calculation is done in the main control system and not in the module.

3 DSP AND ERROR-CORRECTION SECTION

The DSP and error-correction section consists of the 12-bit RAM look-up tables (LUTs), the digital comb filters, and the VXI-interface circuitry. To perform the on-line error-correction process, a known power level is input to the four IF-inputs, the digital data is allowed to bypass the RAM look-up tables. This "actual" data is then compared to the theoretical values that would be obtained at the end of the electronics chain with the known-input power levels. Correct values are calculated and uploaded to the respective RAM look-up tables. The ADC outputs are addresses for the LUTs. Thus when "real" IF signals are input to the module, the log amplifiers attempt to convert the signals according to eqn. 3, the ADCs sample these now-converted dc signals, and the ADC outputs address the LUTs and output the "correct" data to the bus for processing. The "known" power levels are supplied by an Error-Correction Reference chassis described in more detail in reference [8].

Each digital subtractor and comb-filter pair are implemented in a single 12000-gate FPGA which can operate up to 20 MHz. The comb filters are eight-point moving-average filters with a -3 dB cutoff frequency of about 215 kHz assuming a data flow rate of 5 MHz. The input data is 12 bit, and after the subtraction and filtering, 15-bit data is available. The moving average division is implemented by ignoring the bottom three bits and using the upper 12.

The register-based VXI-interface chip-set takes care of essential bus functions and facilitates bi-directional data flow to the module including uploading the corrected data for the LUTs. This part of the module

also provides all of the necessary 5-MHz clock signals to the ADCs, the necessary clock signals to the subtractors, and the clocks for the comb filters.

4 DAC SECTION

The digital-to-analog-converter (DAC) section converts the 12-bit x- and y-axis, and intensity data to analog signals for monitoring at the module's front panel. The x- and y-axis signals' range is ±10 V. The intensity channel is converted to a 0-10 VDC signal. Analog Devices AD767 12-bit DACs are used to perform the conversions. The digital section of the module supplies the proper clock signals and data stream to the DACs. The DAC outputs pass through 200-kHz low-pass filters and buffers before being available at the front panel.

5 TESTING

Preliminary testing of the error-correction technique has been done. These tests used prototype printed-circuit boards and crudely taken data but proved the concept. Uncorrected-position data is shown in Fig. 3. The vertical scale is in dB, and the horizontal scale is in

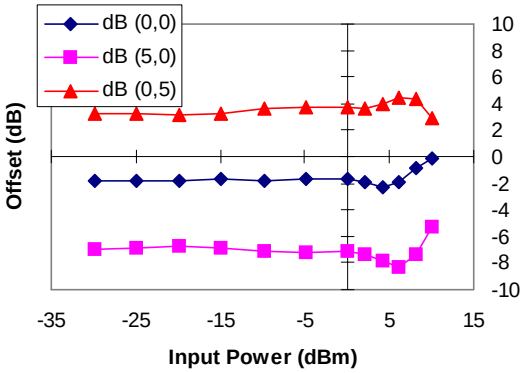

Fig. 4 Graph of uncorrected single-axis position data.

dBm. The input rf signals were offset by 0-dB, 5-dB, and -5 dB. An offset in one of the log amps shifted the curves downward. Important characteristics to note in the graph of Fig. 3 are that the curves exhibit significant distortion and offset over the measured dynamic range of the test. For a properly performing log-ratio system, the lines will be centered about zero offset and be flat. Assuming these errors are caused in general by anomalies such as log amps with differing gains and offsets, dc offsets in the buffers, and ADC non-linearities, error-correcting LUTs will correct the response.

Preliminary error-correction LUTs have been calculated and put into EPROMs. The same system was then tested again and curves plotted in Fig. 3.

The dc offset has been removed, and the distortion in the curves of Fig. 4 have been significantly removed. The top curve is +5-dB offset, and the bottom curve is -5 dB offset.

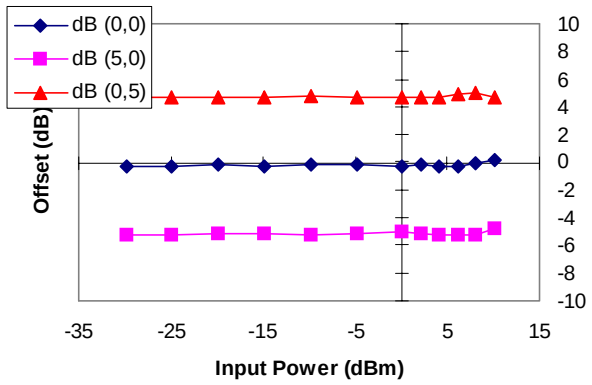

Fig. 3 Graph of error-corrected single-axis position data.

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