# DESIGN OF A VXI MODULE FOR BEAM PHASE AND ENERGY MEASUREMENTS FOR LEDA*

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*Abstract*

Beam diagnostics systems being designed for the Low Energy Demonstrator Accelerator (LEDA) at Los Alamos include beam synchronous-phase and beam energy measurements[1]. The LEDA machine will utilize an RFQ front end operating at 350 MHz, followed by several 700-MHz DTL accelerating structures. Signals from cavity-field probes and beam image-current probes will be down-converted to 2 MHz for phase measurement in VXI modules. Each 2-MHz signal is sampled at 8 MHz with a 12-bit ADC and the resultant data stream is converted into I and Q components which update at a 2-MHz rate. The I and Q signals are then converted to a relative phase measurement. Each VXI module will contain four channels of phase measurement hardware which allow for two channels of differential-phase measurement. Low-noise AGC circuits will accommodate signal variations over a 64 dB dynamic range. An on-board calibration system provides a system absolute accuracy of ±1 degree. DSP filtering allows 200-kHz bandwidth measurements to be made with a resolution of <0.1 degrees over a dynamic range of 46 dB.

## 1 INTRODUCTION

The energy and synchronous phase of the LEDA beam will be determined via a time-of-flight measurement system. Capacitive pick-up probes, as shown in Fig.1 will be placed along the beam line to sample the 350-
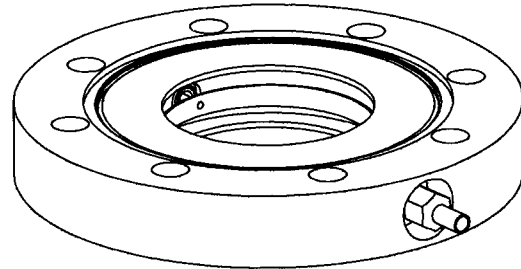


Figure 1 The capacitive probes are designed as integral parts of standard 4.5 in. Dia. Conflat vacuum flanges. Two SMA vacuum-feedthrough connectors support the pick-up electrode.

MHz component of the beam current. The probes consist of a cylindrical electrode of 5-mm length, suspended by two SMA vacuum feedthrough connectors. Three of these probes will be installed on the beamline during the first testing period of the LEDA RFQ. At the nominal accelerator current of 100 mA, over 25 dBm of signal power at 350 MHz is available. These beam signals will be down-converted to 2-MHz IF signals in VXI modules located in the diagnostics equipment racks which are about 60 m from the beamline. In a similar fashion, the cavity field probes will produce high-level signals which are also down-converted.
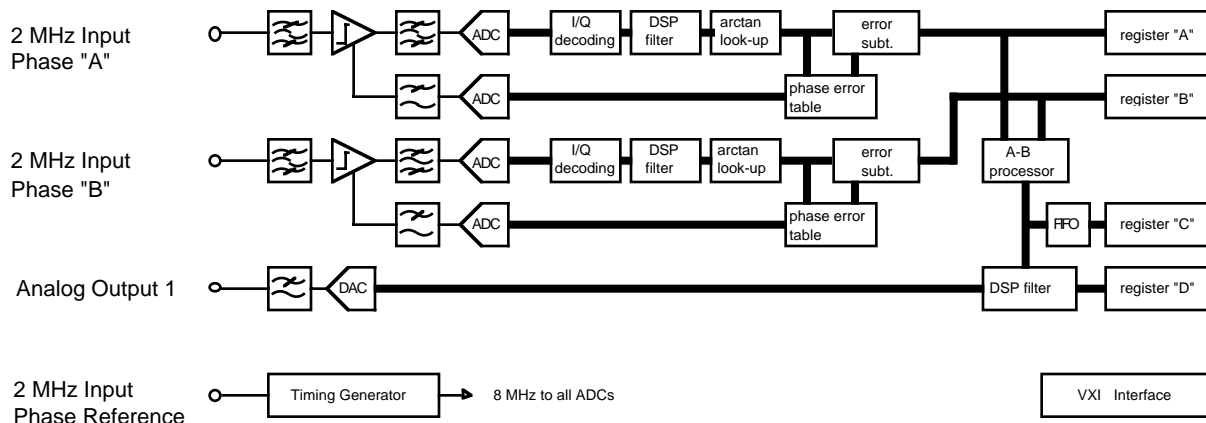


Figure 2 A block diagram of the digital processor. The phase of the analog input is measured and output as a 12-bit word. One LSB corresponds to 0.0879 degrees.

Two types of down-converters are required as the DTL cavities operate at twice the frequency of the RFQ. The 700-MHz cavity-field signals must be down-converted to 2 MHz for comparison with the beam. This requires the generation of two local oscillator frequencies (348 and 698 MHz) from a common 2-MHz reference.

The outputs of the down-converter module mate with a second VXI-based module being designed to measure the phase relationship of the 2-MHz IF signals. This module must have a dynamic range of at least 46 dB (+6 to -40 dBm) and a phase resolution of 0.1 degrees. This phase measurement will have a bandwidth of from dc to 200 kHz, which is greater than the frequency response of the accelerator rf system.

A third module will generate constant-phase 350- and 700-MHz signals for calibration of each phase-measurement channel. The amplitude of the calibration signals will be variable over a 64-dB range.

In this article we describe the salient features of the design of the VXI module which performs the phase-measurement. These features include the digital filtering and I/Q process, the analog AGC front end, and the calibration and error correction technique.

## 2  I/Q PROCESS

The phase of a sinusoidal signal is readily available from its in-phase and quadrature-phase (I&Q) components. The arctangent of the ratio of I and Q gives the angle of the signal relative to the phase of the sampling clock used to define I and Q.

To get the I and Q components, a signal is sampled at four times its frequency , or once every 90 degrees. This results in a repeating pattern of I, Q, -I and -Q values. These values are subtracted appropriately to produce 2I and 2Q. All common-mode errors are consequentially eliminated and low frequency noise (relative to one half the sampling frequency) is attenuated.

We have chosen 2 MHz as our IF which requires a 8-MHz sampling clock. Since our measurement bandwidth is only 200 kHz, we can apply some FIR filtering to the 2-MHz I and Q data streams to reduce the noise by about 50% before the arctangent is calculated. The arctangent function is calculated by a Plessey PDSP16330 Pythagorus processor[2]. This chip uses a look-up table technique to provide a 12-bit 360-degree range with no ambiguity of quadrant. A block diagram of the digital processor is shown in Fig. 2.

In the final design the FIR filter between the I/Q process and the arctangent process to reduces the measurement bandwidth and noise. Unfortunately the PDSP16330 has a fixed 12-bit output, so this filtering will not enhance the measurements ultimate resolution. For this reason an additional programmable FIR filter will follow the arctangent process to be used in cases in which increased resolution is desired. In this case it will be important to guarantee that the phase noise is sufficiently

low relative to the average value, so that the averaging is not done over the inherent discontinuity that occurs at zero and 360 degrees. In other words, the phase of the input signal as seen by the Phythagorus chip should be adjusted to be near 180 degrees at the nominal beam energy.

## 3  THE ANALOG FRONT END

The digital process, which calculates the signal phase, is inherently normalized in amplitude by taking the ratio of I to Q. To maintain the optimum phase resolution, however, it is necessary to use most of the range of the ADC which is 12 bits in our case. We use an AGC circuit to provide a nearly constant output amplitude over a 75 dB dynamic range. This circuit presents the 2-MHz signal to the ADC at a level which is always near its full scale range. Figure 3 shows a diagram of the analog front end (AFE).

The AGC circuit is based on an Analog Devices AD600 part which has an electronically-controlled variable attenuator followed by a 40-dB, fixed-gain amplifier[3]. One of the interesting features of this chip is that the output noise is independent of the gain of the circuit when a single stage is used. Since we require a 46-dB dynamic range we have cascaded two stages of gain control (the AD600 has two stages per package).
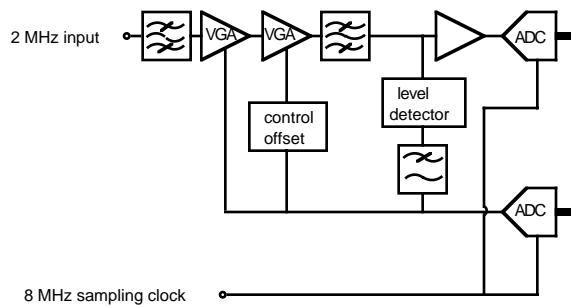


Figure 3  A diagram of the analog front end which includes an AGC circuit with a 75-dB dynamic range.
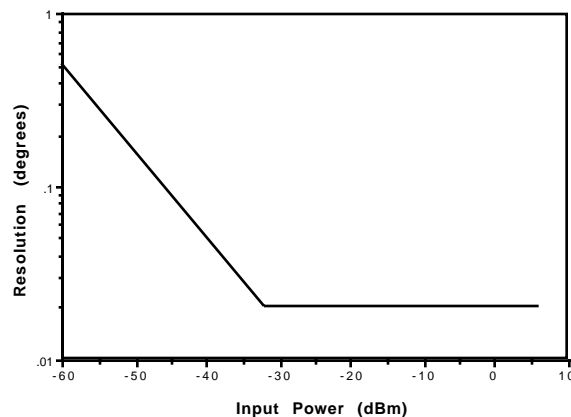


Figure 4  The theoretical phase resolution of the analog front end circuit as a function of signal amplitude for a 400-kHz bandwidth.

The two AGC stages are configured to always use the maximum gain in the first stage and minimum (unity) gain on the second stage, thereby keeping the output noise to a minimum. For signals which are large enough to not require the additional gain of the second stage, the noise level is fixed as a function of amplitude. As the input signal decreases and more gain is required, the noise from the first stage is amplified, along with the signal, by the second stage. A graph of the phase resolution of the AFE as a function of signal amplitude is shown in Figure 4.

The signal that is used to control the gain of the AGC is linear in dB of relative magnitude of the input signal, and is presented to an ADC in addition to the leveled output. This feature will be used to facilitate the phase error correction.

## 4 CALIBRATION AND ERROR CORRECTION

In order to achieve the desired ±1-degree absolute accuracy it will be necessary to correct for the phase shift of the AGC circuit as a function of input signal level as well as provide a periodic calibration of the system to correct for thermal drifts and aging effects. A separate VXI module will generate multiple pairs of constant-phase, 350-MHz and 700-MHz signals whose amplitudes can be programmed over a 64-dB range. These signals will be connected to the beam-phase and cavity-phase probes on the accelerator beamline via phase-stabilized Heliax® cables.

The calibration signals will be stepped through their 64-dB dynamic range while the phase of each digital channel and the associated AGC-control level are logged. The control system will interpolate this data to create an array of phase correction data vs. control level which will then be down-loaded into the phase measurement module. Subsequent phase measurements will then use this correction table to correct the phase data from the Pythagorus processor in real time. A default data set will be stored in ROM to improve the measurement accuracy prior to, or in lieu of, the on-line calibration.

## 5 ADDITIONAL FEATURES

There may be times when it is desirable to analyze a large array of phase data taken just prior to an event such as a fast-protect or beam-abort trigger. A large FIFO memory will be incorporated with each differential-phase channel (two per VXI module) which will store the most recent 200,000 measurements at the full 2-MHz rate (100-ms worth). This data will also be useful for "off-line" FFT analysis, where it is undesirable to take data over the VXI bus at the full 2-MHz rate on multiple channels, simultaneously.

A 12-bit DAC will provide an analog representation of each of the two differential-phase measurements to the front panel. These outputs will be useful during the installation and commissioning of the measurement system. They may also prove to be useful for some beam measurements using analog test instrumentation.

## 6 PROTOTYPE TESTING

A prototype circuit was fabricated which includes the AGC circuits and ADCs for testing. In addition, the digital processor circuits were fabricated using a programmable gate array for decoding the I/Q data stream and interfacing to the Plessey Pythagorus chip. Testing of these two circuits has just begun.

The initial results indicate that the phase resolution of the single-channel system is about 0.035 degrees for a 0-dBm input level versus a theoretical value of 0.02 degrees (defined as one standard deviation). This corresponds to a differential-measurement resolution of about 0.05 degrees which is well within our requirements. A single measurement at an input level of -40 dBm showed a resolution of only 0.2 degrees which is four times higher than the theory predicts. This discrepancy needs further study.

Noise immunity problems with interfacing the two separate analog front end and the digital circuits, combined with some test instrumentation limitations, have prevented us from finishing the characterization of the response over the full dynamic range at this time. A second prototype board which combines all of the required circuitry on a single board is in the process of being fabricated. This is expected to eliminate the interface problems we experienced, and allow us to finish the characterization of the analog and digital front end of the VXI phase measurement system.

## 7 CONCLUSION

The design of a prototype VXI-based beam energy and synchronous-phase measurement system is underway. Low-noise AGC circuits will accommodate signal variations over a 64-dB dynamic range. An on-board calibration system provides a system absolute accuracy of ±1 degree. DSP filtering allows 200-kHz bandwidth measurements to be made with a resolution of <0.1 degrees over a dynamic range of 46 dB. The analog and digital front-end circuitry of the phase-measuring module has been designed and testing is underway. The initial testing indicates that the phase resolution of the module will easily meet the specification at the higher signal levels. Additional testing is underway.

## REFERENCES

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