INTERLOCK AND CONTROL FOR THE RF SYSTEM OF THE ANKA STORAGE RING

D. Einfeld, F. Pérez[+,++], S. Voigt, ANKA, Forschungszentrum Karlsruhe, Germany
M. Humpert, Bonn University, Germany

Abstract

The RF system for the ANKA storage ring has two plants, each plant consists of one 250 kW transmitter at 500 MHz feeding two cavities, with all the peripherals [1]. It has three levels of control: the machine control, the transmitter control and interlock, and the fast interlock. Each one with different response times: 1 sec, 20 msec and 10 µsec, respectively. The first is based on Java language for NT-Windows and LonWorks, the second on an industrial PLC system and the third is hardware electronic. The machine control, controls the whole RF system, but any instruction referred to the transmitter is filtered by the PLC system that executes the action, or not, depending on the status of the interlocks. The fast interlock is running in parallel and shut down the system when a major fault occurs, independent of the others. In this paper we will present the two interlock systems, the general control system of ANKA has already been widely presented elsewhere [2].

1 INTRODUCTION

During the present year the storage ring ANKA is being constructed at the Forschungszentrum Karlsruhe. It will be completely assembled after summer and the commissioning should start in October of this year [3].

To run ANKA, at 2.5 GeV and 400 mA beam current, two RF plants, each one with two cavities powered by a single 250 kW klystron, will be installed [1]. To assure the safe operation of the RF plants a proper control and interlock system should be implemented. At ANKA we have chosen to use an industrial PLC standard, the SPS system from the company BOSCH, for the control and the slow interlock (20 ms). This system will control the RF plant, from the HV power supply up to the interlock signals from the cavities, switching off the plant when any fault occurs. It does not include the low level electronics for the control of the cavities: amplitude, phase and tuning loops. These electronics are provided by Sincrotrone Trieste together with the cavities.

On the other hand, a hardware interlock system will run in parallel for the major faults, acting on a PIN diode switch to shut down the plant in a few microseconds.

[+]On leave from LSB-IFAE, Barcelona, Spain
[++] Email: perez@anka.fzk.de

2 RF PLANT

In figure 1 an scheme of the RF plant with the components and the control structure is shown.

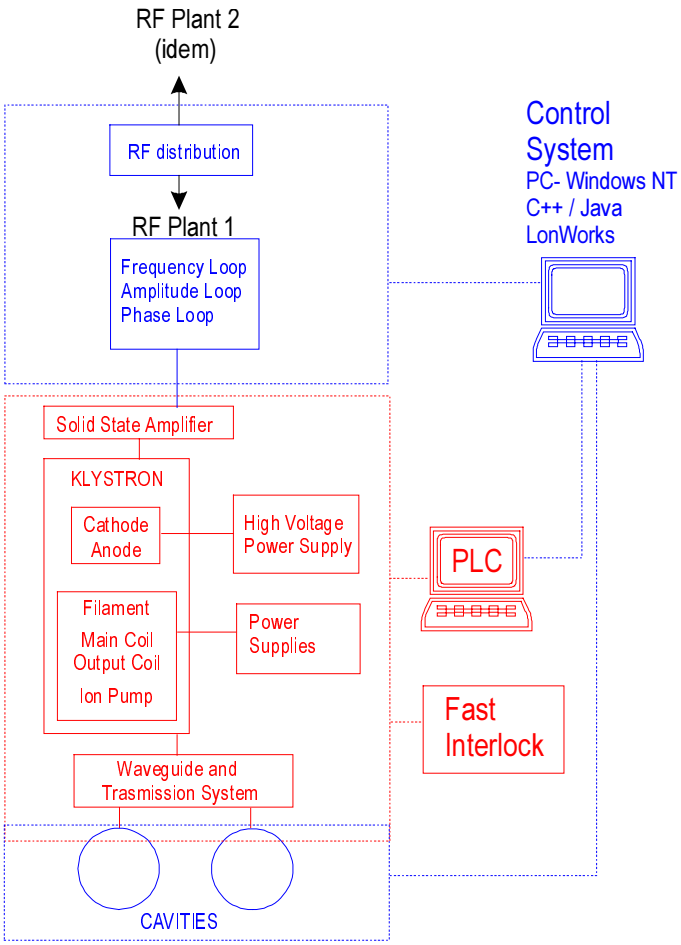

Figure 1: Scheme of the control of the RF system.

The PLC system controls all the components related with the transmitter (pre-amplifier, klystron, HV power supply, small power supplies, ...) and the signals from the waveguide system and the cavities related to the interlock and safety.

The machine control system takes care of the rest of the RF components and controls the transmitter through the PLC system.

3 CONTROL AND SLOW INTERLOCK

The PLC, or local control, is composed of the hardware boards and two software programs, one that processes the signals and executes the appropriate actions, installed in the PLC-CPU; and a second used to visualise this control process.

3.1 Hardware

Different kind of boards are used [4]:

- The CPU ZE200, contains the code that analyse the signals and acts to switch off the RF system.
- The boards to read and write analogue and digital signals, E-ANA, A-ANA, E-24V and A-24V.
- The board for world-wide communication: RS232, Profibus or Ethernet.

They are located in a rack close to the RF plant and they manage more than one hundred signals.

3.2 Software

The process code is mainly a read-out loop with an execution time of around 20 ms. The code compares the incoming signals with the reference ones and in case of mismatch executes the correspondent action:

- Switch off the RF drive
- Switch off the high voltage power supply
- Switch off the complete system

A second code used to visualise the control process has been developed. The aim of this code is to provide a user friendly interface to identify quickly the status of the RF plant and the source of failure, when a fault occurs. The generation of alarms is done automatically.

Figure 2 shows one of the interface panels. The configuration of one of the RF plants is schematically represented: one klystron feeding two cavities through the waveguide system which includes a circulator and a magic tee. The RF power, forward and reflected, at the different points where the directive couplers are located is displayed also in this panel.

The box in the upper side at the centre allows the user:

- Switch On/Off the auxiliaries: small power supplies and other peripheral components.
- Switch On/Off the high voltage power supply and set its operating voltage level.
- Switch On/Off the RF drive.
- Reset the interlocks

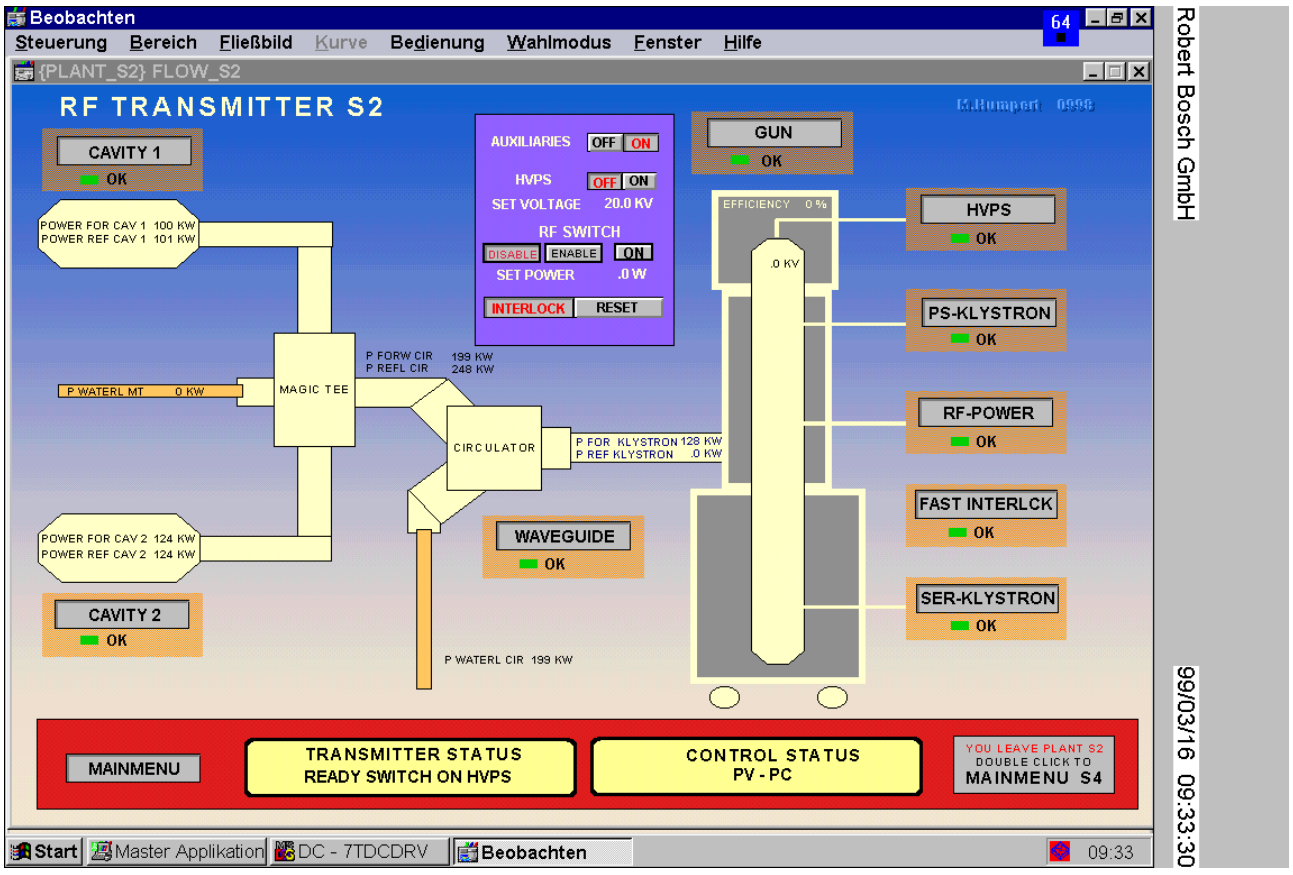

Figure 2: Control panel interface of one of the RF plants

The different interlock signals are grouped in nine groups:

- Ser-klystron: water and air cooling signals
- Gun: gun current and voltage.
- HVPS: high voltage PS interlocks.
- PS-klystron: PS for the coils and vacuum pump.
- RF power: interlock related to excess of RF power.
- Waveguide: cooling and arc detector signals.
- Cavity 1: interlocks of the cavitiy 1.
- Cavity 2: interlocks of the cavitiy 2.
- Fast interlock

The nine small boxes with a virtual LED identify the source of the interlock when a fault occurs (red), or show a correct performance (green). Clicking on one of these boxes another panel opens showing the list of interlock signals and its status: correct (green) or fault (red).

4 FAST INTERLOCK

In parallel to the control provided by the SPS system, we need a hardwire interlock to switch off the system in microseconds when a major fault occurs, i.e. faults that can damage the klystron, the circulator or/and the cavity's window. Figure 3 shows the signals that are included in this fast interlock system

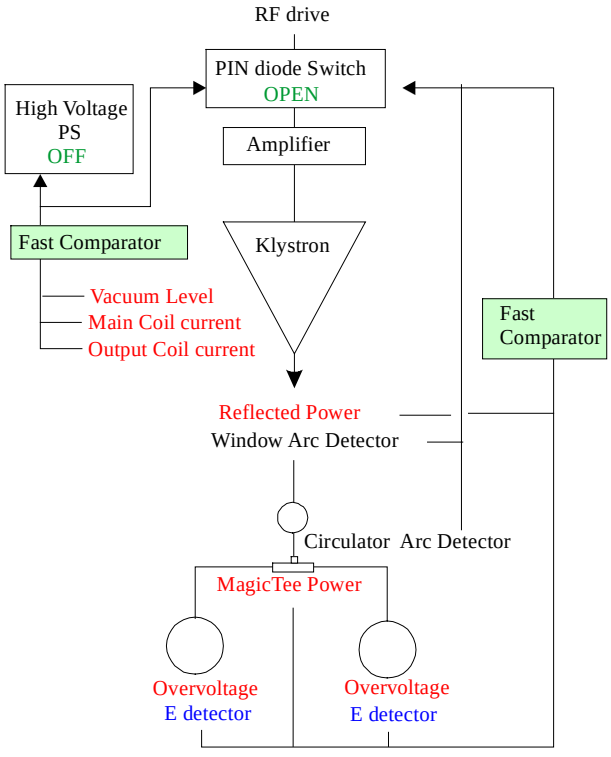

Figure 3: Signals for the fast interlock.

In figure 4 the basic scheme of the fast interlock is shown. The analogue signals are sent to a fast comparator board which compares the signal level to a pre-set value, when the level is over this pre-set value gives a signal to open:

- the PIN diode switch when the fault occurs in the high power RF line; or,
- both, the PIN diode and the HVPS switches, when the fault occurs into the klystron.

The digital alarms from the arc detectors are sent directly to the PIN diode switch. The status of these alarms are accessible from the control panels.

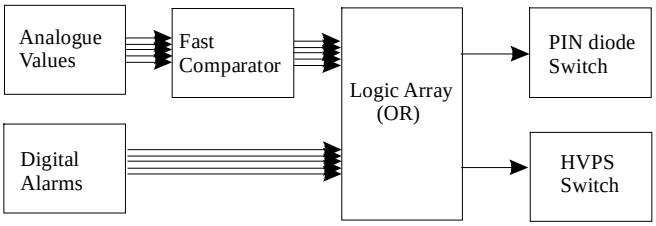

Figure 4: Scheme of the fast interlock.

We will also implement in this fast interlock an electron detector, i.e. an antenna in the cavity's body that, together with an electronic board [5], should be able to detect the flow of electrons just before any sparking occurs inside the cavity. We expect that despite the antenna will located in the cavity's body, it will also help us to protect, in the same way, the cavity's window [6].

5 CONCLUSIONS

The two interlock systems are finished and ready to be tested at ANKA before its implementation on the RF system.

6 REFERENCES

[1] D.Einfeld, F.Pérez, S.Voigt, A.Fabris, C.Pasotti, M.Svandrlik, "Status of the RF System for the ANKA Storage Ring", these proceedings.
[2] B.Jeram, M.Juras, K.Kenda, G.Mavric, M.Peternelj, U.Platise, M.Plesko, R.Sabjan, M.Smolej, G.Tkacik, H.Schieler, "First Experiences with the Control System for the accelerator of ANKA", these proceedings.
[3] D.Einfeld, S.Hermle, E.Huttel, A.Kruessel, M.Lange, F.Perez, M.Pont, U.Ristau, R.Rossmanith, H.Schieler, S.Voigt, R.Walther, A.Weindl, M.Plesko, "Status of the accelerator for the 2.5 GeV light source ANKA in Karlsruhe", these proceedings.
[4] Speicherprogrammierbare Steuerungen, BOSCH Katalog.
[5] Following the DESY design.
[6] M.Ebert, DESY, private communication.