

A SYSTEM FOR PROVIDING HIGH QUALITY TRIGGERS TO EXPERIMENTAL AREAS.*

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Abstract

Many researchers require a high resolution trigger to synchronize their data gathering electronics with the arrival of a synchrotron radiation pulse at their target. At the Advanced Light Source (ALS), this requirement was initially satisfied in a case by case manner by running Heliac cables from the Accelerator Timing System[1] to the various experiment locations. This approach was less than ideal due to poor risetimes, cost and difficulty of running Heliac cables, and the inconvenience of fixed timing. A new system has been installed at ALS that provides the researcher with a high quality, adjustable delay fiducial trigger, and a low level sample of the Accelerator RF (499.66 Mhz). The Ring Orbit Clock (1.523 Mhz) is distributed from the Accelerator Timing System to the various experiment locations using inexpensive twisted pair cable, where it is processed by a Phase Locked Loop Multiplier and High Speed Logic to integrate out noise/jitter and to produce the desired signals. Local drivers provide the researcher with sharp edged robust triggers.

1. INTRODUCTION

High resolution timing signals degrade as they are transported from their source to the timing user. Both high frequency losses and dispersion effects take their toll in the sharpness and accuracy of the product. These effects can be minimized by using higher grade transmission lines, but these lines are both expensive and awkward to handle. Noise, resulting in apparent jitter, is added by ground loop and inductive mechanism to further degrade the signal. Since ALS houses about 6000 square meters of experimental floor, a means of wide distribution, without excessive cost, was needed.

2. CONCEPT

Since ALS timing is strictly periodic, a solution that employs a low resolution fiducial that is processed in the user-end equipment to improve its quality is acceptable.

Clearly, a signal can be distributed at much lower cost if significant degradation can be tolerated, this is the basis of my solution.

Instead of distributing the accelerator RF signal (499.66 MHz), I use its 328th subharmonic, the Storage Ring Orbit Clock (SROC), at 1.523 MHz. This moderately low frequency can easily be distributed over inexpensive twisted pair cable and general purpose fiber optic links.

This signal, along with any phase and amplitude noise that it may have acquired in the course of distribution, is used as a reference signal to a Phase Locked Loop[2,3] (PLL) frequency multiplier that reproduces the desired 499.66 Mhz clock. If the PLL loop filter bandwidth is sufficiently narrow, then the noise integrates out and the quality of the output is primarily dependent on the quality of the PLL Voltage Controlled Oscillator (VCO).

3. DESIGN CONSIDERATIONS

Since low jitter is a primary goal, some effort was put into selection of the VCO. Oscillator jitter is a strong function of the loaded Q of the oscillator resonator[4], so an oscillator employing a high Q resonator was desirable. Since Quartz resonators typically possess Q's a thousand times those typical of LC oscillators, several crystal controlled VCO's (VCXO) were evaluated. A small module from Raltron Inc.[5] was chosen for its low jitter and comparatively low cost.

Although long term stability is controlled by the reference signal, temperature variations in an early prototype produced large phase offsets. These offsets were traced to the temperature sensitivity of the threshold voltage in the digital logic and its effect on the relatively slow risetime of the reference signal, later versions utilize the fully differential features of the ECL logic family to eliminate this phase error.

The loop bandwidth is set at 10 Hz in order to use as much of the short term stability of the VCXO as possible. Such narrow bandwidths can make it difficult to achieve initial phase lock if a simple phase comparator is used. A fairly new dual mode comparator is now available from

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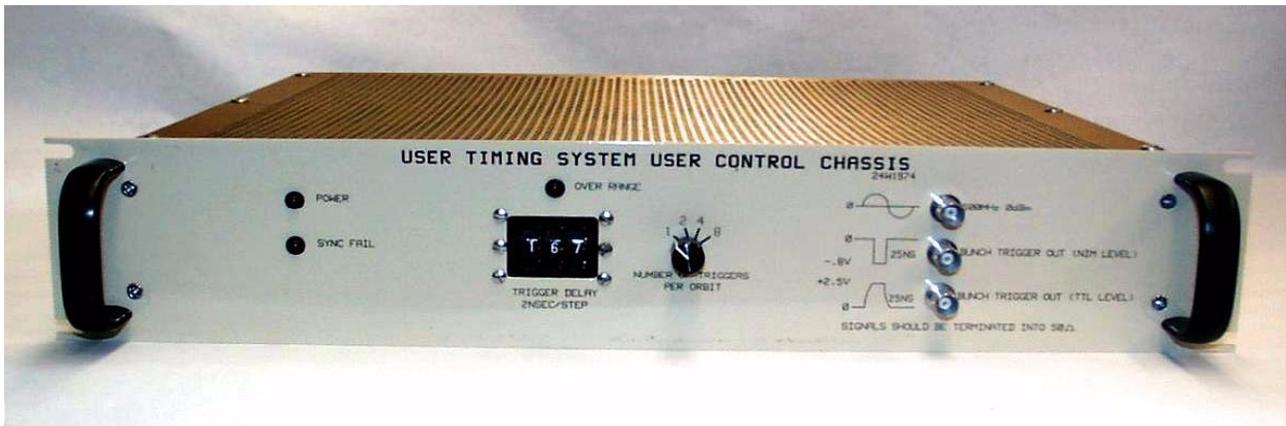


Figure 1

Analog Devices (AD9901) that begins the lock sequence in the frequency comparator mode and automatically becomes a phase comparator after frequency lock has occurred.

This manufacturer has solved a deadband problem that existed in phase/frequency comparators of other designs. An additional feature of the Analog Devices device is its fully differential input and output structure. This allows us to use differential techniques throughout the phase detector and loop amplifier to minimize baseline errors in the analog circuitry.

4. FEATURES

The User Timing Chassis provides two output signals; the accelerator RF frequency (499.66 Mhz.) and a user configurable trigger. The user can select 1,2,4, or 8 evenly spaced triggers per storage ring revolution, and he may position these triggers anywhere in the accelerator period in precision steps of one beam bucket.

The trigger is simultaneously available in TTL, Differential ECL, and NIM. The NIM output features 500 picosecond rise/fall time. All output drivers are designed to drive 50 ohm loads, but are also series terminated to minimize reflections when driving a mismatched load.

Distribution of the reference signal to the various User Timing Chassis around the accelerator is simplified since the only signal that is distributed is a relatively low frequency (1.523 MHz.). The PLL effectively cleanses it of any noise it may have acquired in transit and inexpensive twisted pair wiring is all that is necessary.

5. PERFORMANCE

The output of the User Timing Chassis has been compared with a highly filtered signal from the ALS Master Oscillator to evaluate the phase jitter of the regenerated RF signal. The reference signal was routed across the accelerator through cable trays and used a combination of fiber optic and RS-422 twisted pair transmission. A Tektronics CSA-803 Communications analyzer was used to create a jitter histogram. The analyzer's statistical functions indicate that the RMS jitter measured ~16 picoseconds.

6. ACKNOWLEDGMENTS

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7. REFERENCES

- [1] M. Fahmie, "Design of the Advanced Light Source Timing System," Proceedings of the 1993 IEEE Particle Accelerator Conference, Washington DC, p. 1869
- [2] Motorola Inc., "Phased Locked Loop Design Articles", AR-254
- [3] F. Walls, S. Stein, "Servo Techniques in Oscillators and Measurement Systems", National Bureau of Standards Technical Note 692
- [4] J. Jespersen, J. Fitz-Randolph, National Bureau of Standards Monograph 155, p. 31-40
- [5] Raltron part number VH7126A, Raltron Inc., Miami, FL.

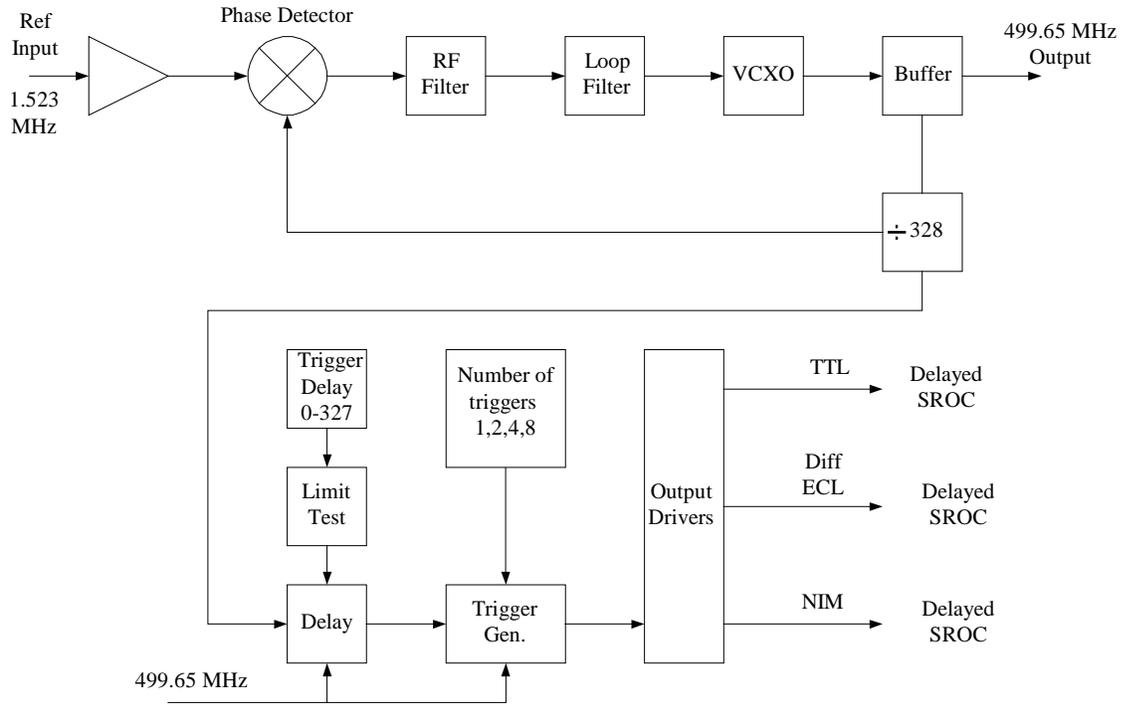


Figure 2 - Block Diagram