RHIC BEAM SYNCHRONOUS TRIGGER MODULE*

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Abstract

The RHIC Beam Synchronous Event System consists of centralized event encoders (one for each collider ring), which operate from the RF clock and the revolution clock provided by the RHIC RF system, and distributed embedded decoders. The Beam Synchronous Trigger Module (V124) is a general purpose 6U x 4HP, VMEbus controlled module that is compatible with the RHIC Beam Synchronous Event System and is designed to provide clocks and triggers for collider data acquisition systems and experiments. The V124 Module contains a separate memory (Bunch Fill Mask RAM) for each channel that is software configurable with the pattern of filled buckets (Bunch Fill Pattern) to permit bunch synchronous triggering/clocking. This module provides eight identical channels that can be configured independently or in pairs, and a buffered RF Clock output.

1 INTRODUCTION

The beam revolution time is approximately 12.78 μs, or 78.196K revolutions/second. The number of RF Buckets (buckets) per revolution per ring is 360. From these data, a 28.15 MHz RF bucket frequency is derived. The Beam Synchronous Event System carrier tracks a varying 14.07 MHz RF clock derived from the RF bucket frequency [1].

The Revolution Clock Event is transmitted when Bucket #1 passes the RF Wall Current Monitor in the 4 o'clock sector. Transmission delays of events are equalized such that each event is received at all locations at the same time. The Revolution Clock Event is decoded and used for clocking the Bucket #1 Delay Counter. The Bucket #1 Delay Counter synchronizes the occurrence of the Revolution Clock Event with the occurrence of Bucket #1 passing by the particular hardware location. This allows the Bunch Fill Mask RAM to always reference the Bunch Fill Pattern to Bucket #1.

Beam Synchronous Event Codes are decoded by the Event Mask Ram to determine if a particular event is used for triggering. Events selected for triggering will be synchronized to the Revolution Clock before triggering a channel. The Beam Synchronous Clock will be extracted from the input data stream so that the RF Clock (2x Beam Synchronous Clock) can be recovered. Recovery will be accomplished by phase locking to the Beam Synchronous Event System carrier and boosting the frequency by a factor of 2. Since only a fraction of RF buckets will contain beam (bunches), recovery of the RF Clock is mandatory for triggering on certain bunch fill patterns [2].

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2 THEORY OF OPERATION

2.1 Phase Locked Loop

The fundamental purpose of the PLL (Phase Locked Loop) is to recover the RF Clock and reduce jitter from the bi-phase-mark modified Manchester serial data stream in the beam synchronous distribution system. The low jitter PLL output clock is then used to clock counters to provide accurate delays and is buffered for further distribution. Sub-nanosecond jitter is guaranteed by the use of an adaptive cable equalizer at the PLL input, and by the use of a differential loop filter design, low noise components, and careful component layout and PCB design. A digital frequency discriminator avoids harmonic lock-up on signal acquisition. An on-board crystal can be selected with a control signal to provide an output when no input signal is available. Prototype jitter was controlled to an RMSΔ of 32 ps over 17 hours with pseudo-random data over the maximum specified cable length.

2.2 Counters

Eight identical trigger channels are resident on each module. Each channel consists of four programmable, cascadable counters: revolution, bucket, trigger and fine.

2.2.1 Revolution Counter

The Revolution Counter is a 16-bit down counter which is loaded with the desired revolution number and whose clock input is the Revolution Clock. This counter can be enabled by:

- A VMEbus Command.
- A Beam Sync Event.
- An External Trigger.
- Paired Previous Channel Fine Delay Enable.

This counter can be reloaded and re-enabled by:

- A Trigger Counter Terminal Count.
- A Bucket Counter Enable.
- Neither (one shot mode)

2.2.2 Bucket Counter

The Bucket Counter is a 10 bit down counter which is loaded with the desired bucket number for delayed triggering after enable and clocked by the recovered RF Clock. This counter can be enabled by:

- A VMEbus Command.
- A Beam Synchronous Event.
- The Revolution Counter Terminal Count.

This counter is reloaded and re-enabled by the Bucket Counter Terminal Count.

2.2.3 Trigger Counter

The Trigger Counter is a 32-bit down counter that is loaded with the desired number of triggers. This counter derives its' clock source from:

- The Bunch Fill Mask Ram Output.
- Bucket Counter Terminal Count.
- Paired Next Channel Bucket Counter Terminal Count.
- No Clock Input (No Halt).

This counter is enabled by the Fine Counter (Delay) Enable (Bucket Counter Enable). This counter is reloaded and re-enabled by the Trigger Counter Terminal Count.

2.2.4 Fine Counter

The Fine Counter (Delay) is a 16-bit delay which is implemented in two 8-bit silicon delay modules. Resolution is 500ps. The (counter) delay is adjustable from 20ns (latency) to 275ns. This (counter) delay is enabled by the Bucket Counter Enable and always disabled on the occurrence of the Trigger Counter Terminal Count. In addition, so that the Fine Counter (Delay) is enabled for only one revolution, the counter can be disabled on the occurrence of the delayed revolution clock. The clock source for this counter is:

- A Fixed Pulse Width (54ns) derived from the Bunch Fill Mask Ram Output.
- A Variable Pulse Width, programmable from 1 to 65536 RF Clocks (35ns to 2.29ms), derived from the Bunch Fill Mask Ram Output.
- A Variable Pulse Width, programmable from 1 to 65536 RF Clocks (35ns to 2.29ms), derived from the Bucket Counter Terminal Count.

2.3 Bunch Fill Mask RAM

Each channel contains 64 bytes (45 used) of RAM which can be loaded with a unique bunch fill pattern. The contents are shifted out a bit at a time at the RF Clock rate. Each bit corresponds to an RF bucket and determines whether that bucket will be used for triggering. The shifting is synchronized such that the sequence starts over at each occurrence of the delayed revolution clock.

2.4 Event Mask RAM

Beam Synchronous Event Codes are decoded and used as pointers into the Event Mask RAM to determine if that code will generate a channel trigger. Each module contains 256 bytes of SRAM that is configured with the channel-triggering pattern. Each bit in each memory location corresponds to a particular channel.

2.5 Timestamp

Each channel provides a 32-bit timestamp derived from the timestamp counter to allow data correlation [3] between data acquired from different systems in widely dispersed locations. The timestamp counter can be configured to count:

- Beam Synchronous Events.
- 1μs clocks derived from the RHIC Event System.

This counter is reset on the occurrence of a RHIC Beam Synchronous Event System SYNC Event. A timestamp (timestamp counter save) acquisition occurs on:

- A Beam Synchronous Event (software configurable).
- The First Trigger pulse of a series of pulses.
- The Trigger Counter terminal count.

The timestamp must be read before another timestamp counter save occurs or the contents will be overwritten.

3 TRIGGERING MODES

This module supports the following triggering modes:

- One or more pulses output every revolution, pulse width selectable, triggered after x number of revolution clocks. Rearm on Trigger Counter Terminal Count.
- One or more pulse output after x number of turns and y number of bunches. Rearm on Trigger Counter Terminal Count.
- One or more pulses output after specified event and y number of bunches. Rearm on Trigger Counter Terminal Count.
- Long Gate. Start is defined by channel 1 and Trigger Counter Terminal Count is defined by channel 2.

- One pulse output continuous for each bunch in bunch fill pattern not to exceed 9.37MHz. Pulse width is 54ns. No Trigger Counter Terminal Count.
- All above modes can be configured as one-shot mode. (No rearm on Trigger Counter Terminal Count).

4 VME INTERFACE

The V124 Module is a VMEbus slave. Status/ID registers (64 bytes), board configuration registers (16 bytes), channel configuration registers (256 bytes), Beam Synchronous Event Mask RAM (256 bytes), and Bunch Fill Pattern Mask RAM (64 bytes) are mapped to VME A16 space on jumper selectable 2K byte boundary (A15..A11). VME data transfers supported are D16 and D08(EO) only.

4.1 Interrupts

Interrupts are supported with a programmable interrupt vector and IRQ level. A nested interrupt structure is employed to service the following hardware interrupts:

- Timestamp Trigger Source.
- Beam Synchronous Event System SYNC Event.
- RHIC Event System Error.
- Beam Synchronous Event System Error.
- Channel Halt.

The RHIC Event System Error and Beam Synchronous Event System Error interrupts are change of status interrupts. Connection or removal of these inputs will cause an interrupt.

4.2 Shared Memory

The V124 shares access to the Beam Synchronous Event Mask RAM between the decoding requirement of the Beam Synchronous Event System interface and the VMEbus. Access to this area of memory by VMEbus requests is allowed only during idle periods of Event System decoding. Highest priority for access is always granted to channel triggering requirements.

Access to the Bunch Fill Pattern Mask RAM is also shared between loading the bunch fill shift register and the VMEbus. VMEbus reads and writes are only allowed during periods that the shift register is shifting out the bunch fill pattern. During loading of the shift register, VMEbus cycles are delayed. Highest priority is always granted to channel triggering requirements.

5 USER INTERFACE

5.1 Front Panel Connectors

The following twin axial inputs are provided:

- Beam Synchronous Event System (1)
- Event System (1)

The following 2-conductor LEMO Model EGG Series 0B connector inputs are provided:

- External Trigger Inputs (4)
- Trigger Outputs (8)
- RF Clock (buffered) Output

The Trigger Inputs, Trigger Outputs and RF Clock output are differential ECL levels.

5.2 Front Panel Indicators

- VME Select – indicates a VME bus access to an address within memory space.
- Beam Synchronous Event System – No Lock
- Event System – Carrier Active
- Trigger Active (8)

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7 REFERENCES

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