SCALPEL: PROJECTION ELECTRON BEAM LITHOGRAPHY*

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INTRODUCTION

Much of the tremendous progress in integrated circuit technology and performance over the past 30 years has been fuelled by the progress in lithography. The ability to print increasingly smaller features has enabled higher speed transistors, higher packing densities and lower power dissipation in CMOS circuits. The productivity of the integrated circuit industry has been on a very steep performance curve, historically improving cost per function of integrated circuits by 30% per year over this period. Roughly half of this productivity improvement is attributable to continuos improvements in lithography technology. The remainder is made up of wafer and chip size increases and circuit design and process innovations.

Leading edge production lithography employs optical projection printing operating at the conventional Raleigh diffraction limit. Generally speaking, the smallest features that can be reliably printed are equal to the wavelength of the light being used. The wavelength of light used for production lithography has decreased historically on an exponential trend curve as illustrated in Figure 1. Light sources have evolved from Mercury arc lamps where they were filtered for the g-line (435 nm) and then I-line (365 nm). Recently, excimer lasers have been introduced as light sources. KrF excimer lasers produce light in the deep ultraviolet (deep uv or DUV) at a wavelength of 248 nm. This source is used currently to produce the most advanced circuits with minimum design rules of 250 nm. Actually, some manufacturers use 248 nm DUV to print transistor gate features as small as 160 nm with resolution enhancement technologies (RET) which allow, in some cases, printing of features somewhat below the conventional diffraction limit.

The issue with optical lithography, which has been characterized by some as a crisis, is also illustrated in Figure 1. Although the progress in optical lithography has been on an exponential improvement curve due to shrinking wavelengths, the slope of the productivity curve for integrated circuits is on a much steeper slope (commonly referred to as Moore's Law). In fact, the two curves intersect at about the KrF (248nm) node for optics and 250 nm node for circuits. This implies, that to make further progress, either new shorter wavelength printing (such as ArF at 193 nm or F_2 at 157 nm) systems must be available sooner than the historical trend (very unlikely) or circuits must be printed below the diffraction limit (which is already beginning to happen). Resolution enhancement technologies or RET allow sub-diffraction printing by controlling the phase as well as amplitude of the light at the image plane in the printing system through the use of phase shifting masks and other "tricks". One other method uses pre-distorted amplitude patterns at the image plane to compensate for some diffraction effects (optical proximity effect correction or OPC). Further, control of the distribution and angle of light (off-axis illumination or OAI) at the illumination aperture can accentuate higher diffraction orders leading to improved performance. These methods are often used in combinations optimized for the particular pattern being printed.

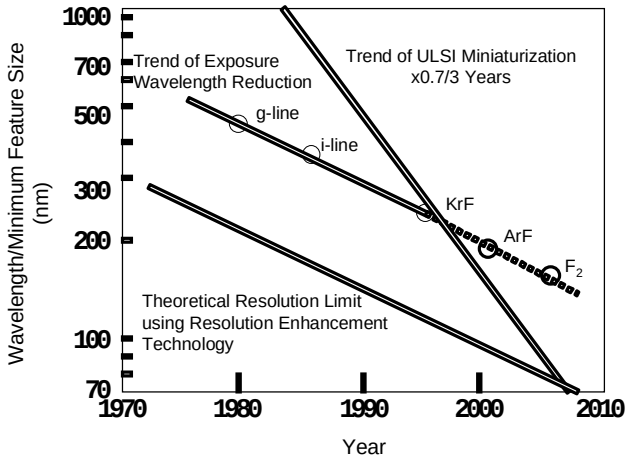

Figure 1. Wavelength trend in optical lithography contrasted with the miniaturization trend in integrated circuits.1

The limit of the improvements offered by RET is the ability to print features at roughly half the wavelength of the light being used, shown as the theoretical limit in Figure 1. The use of these RET techniques can greatly increase the cost of wafer printing and history has shown that printing with shorter wavelengths has proven more economical than employing RET with current technology.

Figure 1 also shows that eventually, the IC productivity curve passes through the theoretical limit even for future optical printing systems. This occurs

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somewhere before the 70 nm circuit generation (currently planned for production in 2009). The next generation of lithography technology beyond optical lithography (NGL) will likely be required for production of the 70 nm generation based on these physical limits. It is also possible that a NGL technology may be employed before to this if it is widely available and offers lower cost of ownership than optical lithography with RET extensions.

A complete technology for printing integrated circuits requires three main elements: the exposure tool, the mask technology, and the resist technology. In IC lithography, an image of the mask (usually reduced by 4 or 5 times) is projected onto the wafer substrate which has been coated with a photo-sensitive material (resist). The solubility of the resist is changed by exposure to light so that a pattern emerges upon development (much like a photograph). The remaining resist pattern is then used for subsequent process steps such as etching or implantation doping. Thus, any lithography technology must have fully developed exposure tool, mask, and resist technologies for it to be successful.

SCALPEL

One of the leading candidates for next generation lithography is SCALPEL® (SCattering with Angular Limitation Projection Electron-beam Lithography).2,3 SCALPEL is a reduction image projection technique which uses 100 keV electrons and scattering contrast. The use of electrons circumvents the limitation of diffraction in optical lithography. The principle is illustrated in Fig. 2.

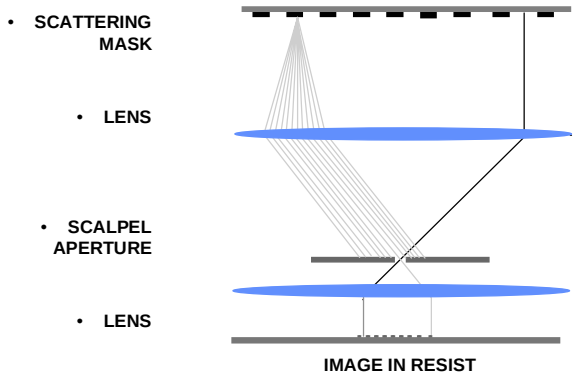

Figure 2. SCALPEL principle.

The mask consists of a low atomic number membrane covered with a layer of a high atomic number material: the pattern is delineated in the latter. While the mask is almost completely electron-transparent at the energies used (100 keV), contrast is generated by utilizing the difference in electron scattering characteristics between the membrane and patterned materials. The membrane scatters electrons weakly and to small angles, while the pattern layer scatters them strongly and to high angles. An aperture in the back-focal (pupil) plane of the projection optics blocks the strongly scattered electrons, forming a high contrast aerial image at the wafer plane. The functions of contrast generation and energy absorption are thus separated between the mask and the aperture. This means that very little of the incident energy is actually absorbed by the mask, minimizing thermal instabilities in the mask.

Imaging Process

In the tool, a parallel beam of 100 keV electrons uniformly illuminates the mask. A reduction-projection optic, in a telecentric doublet arrangement, produces a 4:1 demagnified image of the mask at the wafer plane. Because the features being printed are much larger than the wavelength of the radiation used (λ = 3.7 pm), the full benefits of the reduction ratio are realized, especially in terms of the mask, because imaging is aberration limited, not diffraction limited. This is not the case for conventional optical lithography systems, which, while they are capable of printing very small features, are operating at the diffraction limit. In this non-linear regime, small errors in linewidth on the mask are printed with an effective reduction factor of less than 4:1, sometimes approaching 1:1. The illumination in the SCALPEL system is incoherent, so there are no interference effects. This, combined with the absence of diffraction effects and the high ultimate resolution (~ 35 nm), means that our current tool design will operate relatively linearly for feature sizes down to at least 70 nm, and that the results will be largely independent of the pattern printed. This means that equivalents to OPC (optical proximity-effect correction) are not required.

Writing Strategy

We have chosen to employ a small (1 mm x 1mm at the mask) electron optical field. This is consistent with our strutted mask design and step-and-scan writing strategy. The electron optical field is the same width as the patterned area between the mask struts. In order to achieve high throughput we must increase the effective height of the electron optical field by scanning the electron optical field electronically over an effective field. The effective field height is the same as the length of the patterned area between the mask cross-struts. Die exposure is accomplished by mechanically scanning the mask and wafer through the effective field. This is illustrated in figure 3.

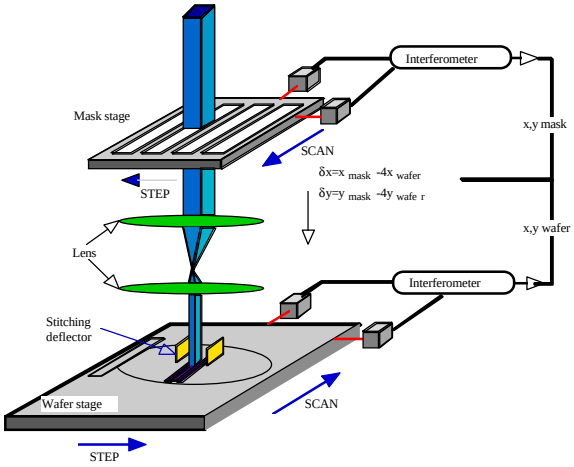

Figure 3 Schematic diagram showing the SCALPEL step-and-scan writing strategy.

The SCALPEL step-and-scan approach confers advantages other than a simplified optical design. The die size that may be printed is not limited by the electron optics, but only by the available mask size and stage travel. This is different from optical step-and-scan systems where the optics must be large enough to illuminate a slit the width of the entire die. Another advantage, particularly in a mix-and-match environment, is that achieving good overlay is made easier. Since the image is effectively assembled from many small pieces, magnification errors or trapezoidal distortions errors can be amortized over a large number of stitching events. Control of the exact stage velocity ratio can be used to stretch or compress the image, and a novel electron optical device can be used to control the magnification and rotation of each individual illuminated area. The use of a small illumination area also allows us to place rigid struts approximately every millimeter to support the thin membrane of the mask, making a robust structure that has minimal susceptibility to pattern placement errors.

The device pattern is segmented on the mask in two dimensions by the struts and must be reassembled or stitched to form a continuous image on the wafer. It is essential to ensure that the critical dimension (CD) of any feature crossing a stitching boundary is maintained to within the tolerances specified by the error budget. The ease with which this may be accomplished is determined by how a feature divided between two stripes is joined. We will employ a seam blending approach to reduce the placement accuracy requirements for controlling feature dimensions across seam boundaries. The edge of each pattern stripe will contain a small overlap region (several microns) in which the pattern features are duplicated on adjacent stripes. These regions are illuminated with a tapered dose profile so that when they are printed, the net dose for these features will be uniform. This method reduces the feature placement requirement for a given critical dimension specification by as much as a factor of five over what would be required if pattern edges were simply butted together.

Results

We have designed and constructed a proof of concept SCALPEL4 system which employs the step and scan writing strategy described above. Along with the exposure tool development, we have also developed the mask and imaging resist technology as a system. To date the masks are made from 100 mm Si wafers with SiN membranes and a patterned W/Cr scattering layer. The imaging resists used have largely been the same as those which have been developed for 248 nm and 193 nm deep UV optical lithography5. Figure 4 is a photograph of our SCALPEL

Figure 4 Photograph of SCALPEL exposure system.system at Bell Labs. It takes up roughly the same amount of space as an optical lithography tool.

Figure 5 shows a scanning electron micrograph of an 80 nm line in positive tone DUV photoresist. This isolated line pattern is part of a gate level transistor pattern.

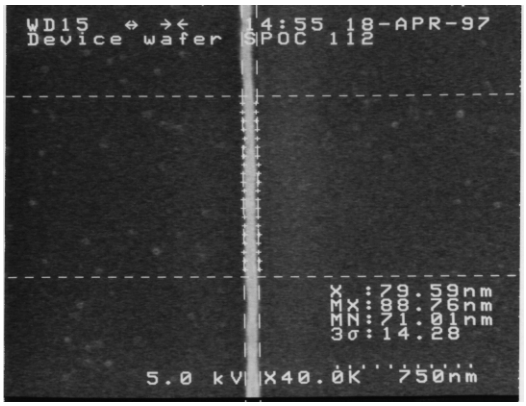

Figure 5. Scanning electron micrograph of 80 nm isolated line gate structure in DUV resist.

Figure 6 shows another example of a pattern typical in integrated circuit designs, contact holes. This pattern is very difficult to reproduce in a diffraction

limited optical system due to its 2-dimensional nature. The image shows an array of 80 nm contacts imaged in a 750 nm thick photoresist film. Quantitative electron microscope measurements showed a depth of focus in excess of 20 microns for a 10% dimensional tolerance. This is nearly 100 times that afforded by today's optical lithography at much larger dimensions.

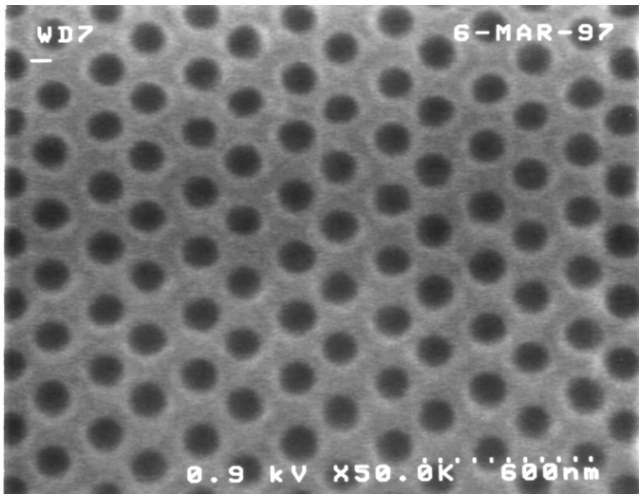

Figure 6 Scanning electron micrograph of an 80 nm contact hole pattern in 750 nm film of DUV photoresist.

SPACE CHARGE EFFECTS

The mutual repulsion of electrons or space charge effect in the beam tends to defocus the beam on average6. This average defocus can generally be corrected by adjusting the focusing lenses. However, the individual stochastic electron-electron interactions cause a blurring of the beam which is not correctable due to its random statistical nature. It is analogous to considering the average position of the electrons to be affected by space charge as well as the distribution about that average. One can re-adjust the average but cannot do anything about the distribution. As one might expect intuitively, the space charge effect is reduced for higher energies, shorter focusing columns and larger beam areas.

Various models and simulations have been employed to predict the effects of stochastic space charge blurring on lithographic image quality in a projection system such as SCALPEL. A primary concern in any lithography system is throughput. The number of wafers that can be printed per hour increases with increasing beam current. However, as the beam current is increased the image becomes blurred by the space charge effect and loses resolution. Thus in SCALPEL there is an inherent trade-off between wafer throughput and resolution. The models predict a somewhat sub-linear relationship between beam current and beam blur. The blur in the beam depends on the total beam current to a power somewhere between 1/2 and 2/3. For maximum throughput, systems such as SCALPEL should be operated in a regime where the performance is dominated by the space charge blur as opposed to aberrations.

Throughput models predict that throughputs of roughly 45, 200 mm diameter wafers per hour are possible on a SCALPEL system assuming a pattern density of 50 % or less (reasonable for critical gate and contact hole layers) and a resist sensitivity of 5-6 $\mu C/cm^2$. This is at least an order of magnitude larger than serial writing electron beam systems but still as much as 50% lower than that of a modern optical lithography system.

COST

The progress in the integrated circuit industry over the last 30 years has been driven by dramatic improvements in cost per function in circuits. For the next generation of lithography technology, whether it is based on optical or electron beams, must be cost effective in order to be consistent with the industry expectations. In estimating the cost of printing a lithographic pattern on a wafer, there are three main elements: 1) the cost of operating the exposure tool which is proportional to its price divided by its throughput, 2) the mask cost which is the price of the mask divided by the number of wafers to be printed with it, and 3) the cost of the resist materials and development of the image. The choice of the next generation lithography technology is likely to be made on this basis rather than on strictly on technical grounds since there are several alternatives that can achieve similar results but at different degrees of difficulty and cost.

In comparing SCALPEL to advanced optical lithography on the basis of estimated costs, the throughput of an optical tool may be as much as twice that of a SCALPEL tool but is likely to cost twice as much making the first term roughly equal. The resist and processing costs slightly favor SCALPEL since some complexities such as antireflective coatings under the resist are not needed. The most significant difference is in the mask costs. SCALPEL operates in a linear printing regime and therefore uses a true 4:1 representation of the circuit pattern on the mask. In sub-wavelength optical lithography, the masks must be much more complex to compensate for diffraction effects in printing. The mask cost will be the dominant factor in the overall costs and thus SCALPEL technology will have a significant advantage over optical lithography in the sub-wavelength regime.

SUMMARY

Even though virtually all integrated circuits over the past 30 years have been made using optical lithography, the limits of its usefulness are on the horizon. From the point of view of the physics of the image formation process, it is difficult to imagine practical processes operating at feature sizes at or near half the wavelength of the exposure system. The exposure wavelength trend has been to tend to ever smaller ultraviolet wavelengths but at a pace slower than the feature size trend for integrated circuits. Therefore, both the imaging mechanisms and industry timing indicate that a new disruptive lithography technology will be needed sometime after about 2003. We have developed SCALPEL electron beam lithography to the point where the basic functionality has been shown. Our efforts over the next few years will be to develop the exposure tool, mask and resist technology to the point of commercial introduction consistent with that timing. Ultimately, relative costs of lithography alternatives will determine the successor to current optical technology. The projections are that SCALPEL will operate at a significant cost advantage to sub-wavelength optical technology and other contenders for next generation lithography. Therefore, we feel that SCALPEL is likely to be the industry choice for 100 nm era circuits and beyond.7

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[7] For further information, see our web site at http://www.lucent.com/SCALPEL .