MECAR (Main Ring Excitation Controller and Regulator): A Real Time Learning Regulator For The Fermilab Main Ring Or The Main Injector Synchrotron.

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ABSTRACT

The real time computer for controlling and regulating the FNAL Main Ring power supplies has been upgraded with a new learning control system. The learning time of the system has been reduced by an order of magnitude, mostly through the implementation of a 95 tap FIR filter in the learning algorithm. The magnet system consists of three buses, which must track each other during a ramp from 100 to 1700 amps at a 2.4 second repetition rate. This paper will present the system configuration and the tools used during development and testing.

1. INTRODUCTION

The Fermi National Accelerator Laboratory Main Ring is used as an injector to either the Tevatron or the Antiproton Source. The Main Ring accepts 8 GeV beam from the Booster and accelerates the beam to either 150 GeV for use in the Tevatron or to 120 GeV for antiproton production. MECAR is an upgrade consisting of new computer hardware, current sensing equipment, and software.

The power system consists of three buses: one dipole bus with twenty-five power supplies and two quadrupole buses each having four supplies. Each power supply is a filtered 12 pulse SCR converter rated at ±850 V and 3 KA. The dipole bus has a total inductance of 6 Henrys and a resistance of 6 Ohms. Each quad bus is .2 Henry and 1 Ohm. Both quadrupole buses are required to track the dipole bus while the current is ramped from 100 amps to either 1,360 (120 GeV) for the production of antiprotons, or 1,700 amps (150 GeV) for Tevatron injection. MECAR provides reference waveforms for all the power supplies and performs the real time current feedback for all three magnet buses. In addition, MECAR executes the cycle to cycle learning algorithms to further minimize regulation errors, and interfaces with the accelerator control system.

In about three years the Fermilab Main Ring will be upgraded to a new synchrotron known as the Main Injector. MECAR will be relocated to the Main Injector when needed and has been constructed to be compatible with both machines.

2. TRANSDUCTOR HARDWARE LAYOUT

Current signals are provided to MECAR through a set of DCCT's and subtraction electronics similar to other current regulation systems at Fermilab[1] . These DCCT's are temperature stabilized and have an initial offset accuracy of <100 ppm with a long term drift stability of ≤10 ppm. Dual transductors are installed for redundancy (see Figure #1). For the bend bus, a high resolution current error signal is generated by subtraction electronics taking the difference between the transductor signal and the output of a temperature stabilized D/A converter. With a gain of 100, this 21 bit equivalent signal is sent back to MECAR. The quadrupole current is measured with a difference transductor which subtracts the quad current from the bend current. This high resolution signal is used to regulate the quad bus current.
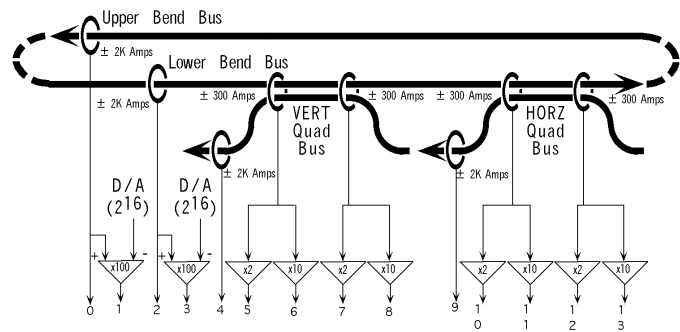

Figure #1   Bus Transductor Configuration

3. MECAR COMPUTER HARDWARE

The MECAR computer is made up of a 20-slot, 6U VME crate and various VME cards. A short description of the more important VME cards follows:

- Five CPU Boards: 25MHz 68040, 16MB RAM, ethernet
- Two Timer Boards: Clock decoding, timing and delay counters, 4 interrupt channels, in-house design
- Two Digital I/O Boards: 64-bit and 48-bit digital I/O boards, 8-bit programmable ports
- ADC Board: 16-bit, 64 Channel, 19uSec conversion time per channel, VME interrupt ability
- Power Supply Link Receiver and Transmitter Boards: 10Mbit, serial, unidirectional, proprietary data link, in-house design

It should be noted that some difficulty was encountered using the 68040 floating point processor in real time. Unmaskable interrupts are generated in response to simple underflows and overflows. These interrupts cause unacceptable performance degradation and even real time failure. The problem must be solved using explicit bounds checking throughout the real time signal processing.

4. MECAR SOFTWARE

4.1. Software Development Tools

Each of the CPU Boards are running Wind River Systems, Inc. VxWorks Real Time Operating System version 5.1.1. The VxWorks Development platform is an HP 9000 Model 735 Workstation. The version control for the C and 68k assembly language source code is done using the UNIX Source Code Control System (SCCS).

4.2. Subsystem Communication

Communication to MECAR is supported through two different mechanisms. The first is via Remote Procedure Calls (RPC), a protocol which is supported by VxWorks. An RPC driver Virtual Instrument (VI) interface was developed in-house for National Instrument Corp.'s LabVIEW®. LabVIEW's powerful and efficient environment was used extensively during development for reading and setting all manner of parameters. Many VI's have been made for engineering development, control, and diagnostics. Once MECAR becomes operational, LabVIEW VI's will only be used for engineering parameters and some debugging functions.

The second communication mechanism is the Accelerator Controls Network (ACNET). ACNET is a proprietary communication protocol which is used at Fermilab for all Control and Operational network communications. ACNET software is running in one of the five CPU boards in MECAR. Server RPC software written to support LabVIEW VI's during development is reused, whenever possible, by making client RPC calls from ACNET routines. Client RPC's are used by ACNET routines to communicate with the other four CPU boards in the MECAR VME crate. The RPC's use a Shared Memory Network supported by VxWorks, which is a TCP/IP network running over the VME backplane.

All real time communication between the CPU boards is done using shared memory over the VME bus.

4.3. MECAR Timing / Synchronization

The sample rate of the real-time code in MECAR is 1440Hz. The sampling interrupt is generated by a software controlled oscillator (SCO) which is phase locked to a 720Hz event on the accelerator clock system (TCLK). A phase-lock loop (PLL) is used to isolate MECAR from variations in the accelerator clock.

4.4. Signal Processing

A parallel 4 stage pipeline architecture is used for real time signal processing (see Figure #2). Assembly language is used to achieve 50% bandwidth utilization. The first stage is a hardware MADC triggered directly by the Phase Lock Loop (PLL). A VME interrupt from the MADC starts the second stage which executes in the System Program And Measure (SPAM) processor. System program information from the Accelerator Control System specifies all current waveforms. These programmatic signals are compared with transductor measurements from the MADC to determine the error in each of the 3 guide field buses.

These error signals are passed on to the third stage which executes in each of the 3 bus controller processors

(BEND, HORZ, and VERT) simultaneously and independently. Here regulation is accomplished with feedback and feedforward learning. The drive voltage is dispersed to successive tiers of power supplies in such a way as to minimize the voltage to ground seen by the magnets, and minimize reactive power, but allow sufficient slew time.
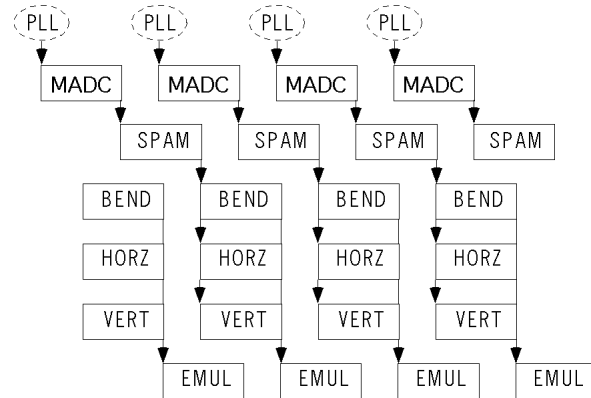
Figure #2   Execution Pipeline (time -->)

The last stage is used for development, diagnostics, and monitoring. Execution begins in the emulator (EMUL) processor after it has received an interrupt from each of the three Bus Controllers and basically emulates the response of the magnet load and power supply system for testing purposes. This load emulation has proven to be invaluable during development and commissioning.
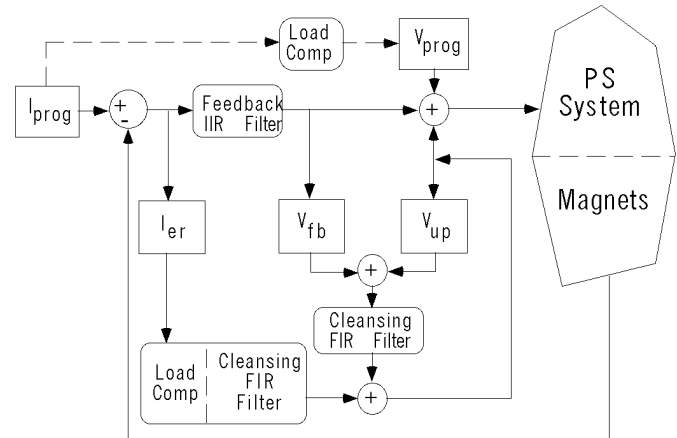
4.5. Regulation

Figure #3   Control Signal Flow

A precalculated feedforward voltage program (Vprog in Figure #3) will drive the load to within ±1% of the reference waveform. The feedback loop (outer loop including the IIR filter in Figure #3) will bring it to within ±500 ppm. The feedforward learning (inner part of Figure #3) further reduces the error to ±30 ppm of maximum current. Feedforward learning is done by adding an "update" waveform, $V_{up}(t)$, to the power supply voltage drive. It is incremented each accelerator cycle by the sum of two signals: the real-time

voltage feedback applied during the previous cycle plus the voltage calculated to compensate for the measured current error. High frequencies of the new update waveform are attenuated for stability purposes with a FIR filter. Mathematically:

$$V'_{up}(t) = F_{FIR}(V_{up}(t) + V_{fb}(t) + L\dot{I}_{er}(t) + RI_{er}(t))$$

where the new update $V'_{up}(t)$ is calculated from the old update $V_{up}(t)$, the old feedback $V_{fb}(t)$, and the old error $I_{er}(t)$.

4.5.1. Feedback and Learning Interaction

Feedback can react to non-repetitive transient errors, but it can't anticipate errors; it has a finite phase delay. Feedforward learning, on the other hand, can anticipate errors, but only repetitive ones; it has no phase delay. When feedback and learning are connected properly, system stability separates into two domains: the time continuous domain for feedback, and the cycle to cycle iteration domain for learning. From a feedback stability point of view, the only effect of the learning is that the feedforward voltage program happens to be different on successive cycles. Within a cycle, on a time continuous basis, feedback stability is governed by classical theory. From a learning point of view, the new corrective learning signal is determined from the previous error signal. This error signal resulted while the previous feedback was present. Therefore, this new corrective signal must be applied with the previous feedback signal. The correction signal that is applied to the next cycle is the sum of the calculated voltage needed to correct the previously measured error and the corresponding previous feedback signal.

4.5.2. Feedforward Learning Stability

If the load is well behaved and completely predictable out to the Nyquist frequency, then a load compensation filter, if sufficiently accurate, will render the learning system absolutely stable. However, this is not the case with a large magnet system having multiple power supplies and stretching out over 4π kilometers. As different power supplies turn on during the ramp cycle, changing transmission line effects of the distributed magnet system make the high frequency behavior of the load intractable. Simply attenuating these frequencies in the load compensation and feedback signal is insufficient to make learning stable, because even the smallest error leakage will eventually accumulate in the updates and run away. The accumulated voltage correction must be "cleansed" of these frequencies on a regular basis. It can be shown that if transmission of the cleansing filter, $\alpha(f)$, satisfies:

$$\alpha(f) < \left| \frac{Z_{load}(f) + Z_{gain}(f)}{Z_{load}(f) - Z_{comp}(f)} \right|$$

for all frequencies at which the load is unpredictable, then the learning will be stable. Where $Z_{load}(f)$ is the actual load impedance, $Z_{gain}(f)$ is the feedback IIR filter and gain impedance, and $Z_{comp}(f)$ is the load compensation impedance.

4.5.3. Use of FIR Filters for Learning

Finite Impulse Response filters are ideal for feedforward learning because they can be implemented with absolutely no phase distortion or delay of any kind, by making them symmetric in the time domain. Currently a basic 95 tap FIR filter (see Figure #4) is being used to insure learning stability. A roll off at 30 Hz is chosen to match the frequency at which transmission line modes start to dominate in the bend bus.

5. TESTING

Due to the desire to maximize the physics output of the accelerator complex during the past six months, very little time has been available to test MECAR with the power supply system. However, with the time that has been available, MECAR has successfully operated and accelerated Main Ring beam. During these tests the learning algorithms have shown to be effective in 1 or 2 machine cycles. This represents a 10 fold decrease in learning time over the present system.
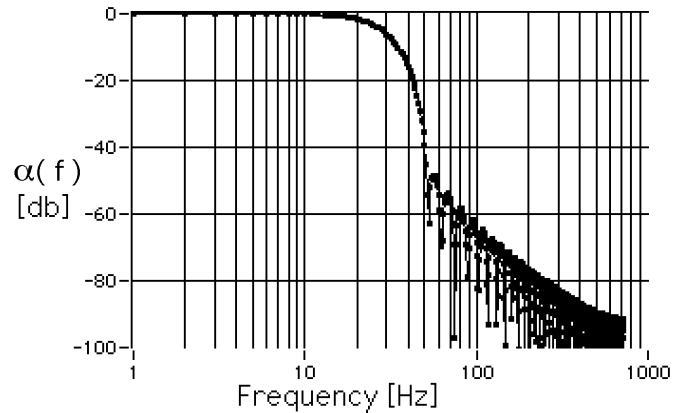

Figure #4 Cleansing FIR Filter Frequency Response

6. CONCLUSION

It has been proven that it is possible to build a feedforward learning controller that essentially learns in one repetition cycle. With attention to load filter accuracy and cleansing filter bandwidth, one can make such a system absolutely stable.

7. ACKNOWLEDGMENTS

8. REFERENCES

[1] S. Hays, D. Wolff and H. Pfeffer Fermilab, "Power Supply Regulation Systems Installed in the Fermilab Accelerators" **IEEE Nuclear Science Symposium** November 1991