DSP BASED DATA ACQUISITION FOR RHIC*

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Abstract

A flexible data acquisition platform has been developed for use in RHIC beam instrumentation systems. By incorporating a floating point digital signal processor (DSP) and standard input/output modules, this system can acquire and process data from a variety of beam diagnostic devices. The DSP performs real time corrections, filtering, and data buffering to greatly reduce control system computation and bandwidth requirements. We will describe the existing hardware and software while emphasizing the compromises required to achieve a flexible yet cost effective system. Applications in several instrumentation systems currently under construction will also be presented.

I. INTRODUCTION

Like other modern accelerators, RHIC will be well instrumented at commissioning[1][2]. Also, the design philosophy embodied in the various beam instrumentation systems places digitizers early in the signal processing chain[3]. To deal with the resulting data rates, most instrumentation systems will include a digital signal processor followed by a memory buffer that is shared with the control system. This DSP provides the following functionality:

- Filtering that can decrease the data bandwidth to the control system
- Corrections and calculations that decrease the computational load on the control system
- Local circular buffer management to provide a flight recorder
- Software flexibility to present data from various I/O modules in a consistent manner

The decision of how to split functionality between the DSP and the control system is subjective. When allocating functionality to the DSP we use the general guideline that the DSP system is not to be treated as a peer to the control system processors. Rather, the DSP system is viewed as a replacement for hardware that simply provides data to shared memory on a bus slave board. As a result, the DSP board described below is not a bus master, and the software for the example application is limited and simple. In fact, much of this functionality could be obtained with field programmable gate arrays, but the current development tools did not allow the flexibility that we desired. This situation will change in the future, and for higher bandwidth instrumentation, a hardware dominated system will be considered. So far, our only use of a hardware based system is in the injection profile monitors where commercial image processing boards extract information from four simultaneous video data streams[4].

II. DSP BOARD DESCRIPTION

This section describes the hardware architecture and performance of the DSP based data acquisition module. The module is physically incorporated on a single width 6U VME standard printed circuit board It may be installed into a standard VME crate, or as one-half of a VXI module, as has been done for this application. Figure 2 illustrates the block diagram of the design. Listed below are the highlights of the board which will be described in order.

- Motorola DSP96002
- VME/VXI interface
- 4Mbytes Static RAM
- 128Kbytes FLASH memory
- Accepts 4 Industry Pack (IP) Modules

The centerpiece of this module is the Motorola 32 bit floating point DSP. The DSP boasts 16.5 million instructions per second (MIPS), and 49.5 million floating point operations per second (MFLOPS). In addition to its strong performance characteristics, it provides two 32 bit I/O ports, shown as port A and port B in figure 1. These two ports permit independent handling of the raw data input from the Industry Packs (port B), from the post-processed data awaiting upload through VME in the static memory (port A).

The module provides a full 32 bit slave interface which conforms to the IEEE-1014-87 specifications. The necessary VXI registers have also been implemented for compatibility in a VXI environment. The VME bus has full read and limited write access to the Static and FLASH memories. Arbitration for the local bus is performed between the DSP and VME bus with the DSP having higher priority. This priority scheme was chosen to allow the greatest overall DSP performance possible. Due to the asynchronous nature of VME transfers, it remains unaware of this arbitration and only it's acknowledge signal is delayed until it can gain access to the local bus

The on-board memory consists of both static ram and flash memory. The static ram has multiple sources and is packaged in 64 pin zigzag JEDEC standard modules,

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permitting easy installation and upgrade. A maximum of four of these memory modules may be installed in sizes of 256kbytes, 512kbytes, or 1Mbyte each. Two size identifying pins on the memory modules themselves allow the hardware to automatically configure itself to the installed size. Since static memory can become expensive the DSP board allows installation of a single 64kbyte memory module for cost sensitive applications, or the installation of four 1Mbyte memory modules for more demanding applications. The on-board flash memory provides a nonvolatile area for program instructions and any necessary permanent coefficients, etc. It provides eight lockable sections, so that a core level program may be locked into a section to prevent inadvertent changes.

What helps makes this board a versatile data acquisition board is its use of a mezzanine cards known as Industry Pack Modules. This interface was developed by Greenspring Computers, and provides a versatile, modular approach for implementing a wide range of I/O, control, interface, analog and digital functions. Up to four of these Industry Pack Modules may be installed on the DSP board while still occupying only one VME slot.

The performance of the DSP board can be characterized by the performance of the DSP itself, along with its I/O throughput with both the SRAM and the Industry Packs. Some performance issues of the DSP itself were listed above, and now the I/O performances of the DSP that were accomplished will be mentioned. On port A of the DSP are the SRAM modules. They are accessed with a single wait state giving a maximum throughput of 42Mbytes/sec, and may have internal access times up to 45ns. On the other port are the Industry Pack Modules. The maximum throughput achieved with the Industry Packs at 8Mhz is 5.3Mbytes/sec. This can be doubled to 10.6Mbytes/sec with a double wide industry pack. The Industry Pack specifications also specifies (preliminary) a 32 Mhz interface, which has been implemented on two of the slots, giving a throughput of 12.8Mbytes/sec. (25.6Mbytes/sec for double wide Industry Pack).

III. APPLICATION EXAMPLES

The number of digitizer channels serviced by a single DSP board depends on the digitizing rate and the complexity of the signal processing algorithm. Examples are summarized in Table 1. The Injection position monitor system is in production and will be commissioned beam in late 1995. A prototype of the collider ring position monitor module has been tested but production will not begin until 1997. A loss monitor module has not yet been constructed. The two variations of position monitor systems will be described. These two systems share the same sampling detector design, but use different digitizers, different timing system interfaces, and run different DSP software. Nevertheless, the results are presented to the control system in identical data structures. In fact, these data structures are similar to those of the RHIC control system's general purpose digitizers[5].

Table 1: Typical Data Rates

Application	Digitizer Channels per Module	Peak Digitizer Sample rate (Sa/s)
Injection Line Position monitors	24	30
Ring Position Monitors	4	78k
Ring Loss Monitors	8	20k

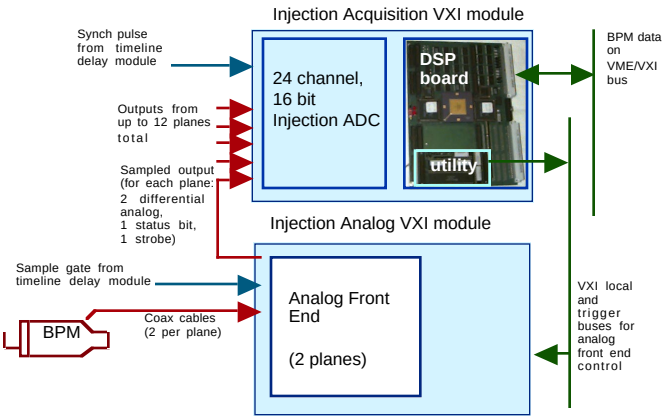

Figure 1. Diagram of Injection Line Modules

A. The Injection Line Position Monitor

The electronics for this system consists of the two VXI modules shown in Figure 2. Because of the low data rate in the injection line, a single DSP board can service multiple analog VXI modules and does not provide any averaging. Software for the injection line application can be summarized with the following routines:

- The acquisition routine runs upon interrupt from the digitizer (about 30 Hz):
  - Raw values are corrected to 3rd order.
  - Position and charge for each bunch are calculated.
  - The buffer pointer and a bunch counter are updated.
  - Results are stored in a circular buffer residing in shared static memory.
- The housekeeping routine is run on interrupt from timing system:
  - Values of the buffer pointer and bunch counter are stored (part of scheme to synchronize buffers of geographically separated modules).

- Changes to settings are read from shared memory and applied.
- If the appropriate bit is set, a self calibration is performed.

B. Collider Ring Position Monitor

Because of the high data rates (turn by turn) of the ring system, a DSP board only services four digitizing channels. Also, the 110 ns bunch spacing in the ring requires that the DSP software be synchronized to the beam synchronous timing system. This special timing interface resides on one Industry Pack while the 4 channel, 16 bit digitizer fits on another. The two planes of analog front end reside in the front of the C-size VXI module. A block diagram of this module is shown in Figure 3. The DSP software for this module can be summarized as follows:

- The acquisition routine runs upon interrupt from the digitizer (about 78 kHz):
  - This routine is similar to injection line acquisition routine, but in addition, the calculated values and their squares are both accumulated.
- The statistics routine is run on interrupt from the timing system (usually at the synchrotron frequency - a few hundred Hz max.):
  - Average and variance of charge and position are calculated.
  - Results are stored in a separate circular buffer.
  - Pointers and counters relating to this circular buffer are updated.
  - The accumulators are cleared in preparation for the next averaging period.
- housekeeping routine is similar to the injection line version

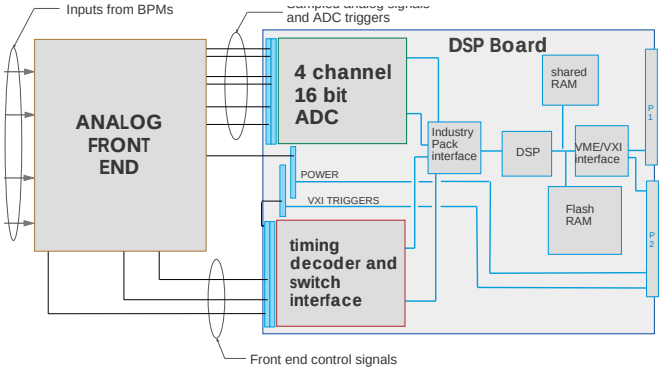

Figure 2. Diagram of Ring Module

IV. FUTURE DIRECTIONS

In addition to investigating competing processors, we are also considering available logic synthesis tools and their viability for higher bandwidth applications. High level development software may soon allow the DSP to be replaced with field programmable gate arrays.

VXI packaging is proving to be restrictive and expensive for some applications so replacement of the VXI interface by a serial bus connection is being investigated. IEEE-P1394 is a likely candidate and provides the following features:

- 100, 200, or 400 Mbits/s bandwidth
- asynchronous or isochronous data transfer
- simple memory mapped interface (64 bit address)
- maximum of 4.5 meters between nodes is standard - extend to much longer distances with cable upgrades and/or bridges
- cheap ($50/node)

The evaluation of the P1394 serial bus will proceed as follows:

- Phase 1: existing DSP board will be a test-bed for a 1394 Industry Pack
- Phase 2: new IP carrier board with 1394 built in

V. ACKNOWLEDGMENTS

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VI. REFERENCES

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