FERMILAB BOOSTER LOW LEVEL RF SYSTEM UPGRADES

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Status of and plans for upgrades to the aging Booster Low Level RF phase and frequency control system are described. The central feature of the new system is replacement of the existing analog voltage controlled oscillator (VCO) with a direct digital synthesizer (DDS) operating directly at the Booster 37-53 Mhz frequency. This eliminates historically chronic problems with VCO frequency drift and setting inaccuracies. Initial implementation consists of the DDS operating under digital signal processor (DSP) control to generate the open loop frequency sweep profile and to close the beam phase-locked frequency loop. Further iterations will bring synchronous phase control, RF station counter-phasing operations at injection and extraction times, and the Booster to Main Ring beam transfer synchronization and phase-lock process under precise and programmable digital control. These improvements will facilitate and provide the enhanced flexibility for features, including new transfer synchronization options, expected to be necessary for continued high intensity operation from now into the Fermilab Main Injector era.

I. INTRODUCTION

The rapid cycling Fermilab Booster operates on a 15 Hz sinusoidal magnetic cycle to accelerate protons from 400 MeV to 8 GeV. At a harmonic number of 84, the Booster rf must sweep from 37.8 to 52.8 Mhz during the 33.3 msec acceleration interval, exhibiting a maximum *df/dt* of 1.74 Mhz/msec at 4 msec into the cycle. Figure 1 shows selected Booster parameters as a function of time in the cycle. The Low Level RF (LLRF) System provides to the high power systems, each driving one of 17 accelerating cavities, a global rf reference signal at the proper frequency and phase to control beam energy during acceleration and to synchronize bunch-to-bucket transfer of the beam to Main Ring. Programmable feedforward curves and real-time beam feedback signals function within the LLRF to provide stability to the acceleration process and facilitate operator control of radial beam position during the cycle.

II. MOTIVATION FOR THE UPGRADE

The operational LLRF system in Booster today exists in much the same form and utilizes the same hardware as described by Meisner [1], Kerns [2], Jachim [3], and Ducar [4] over the past 16 years. This equipment has served the Booster well for as much as 20 years, but obsolete components now present maintenance problems and the system lacks features and flexibility important for present high intensity operation. Figure 2 is a functional diagram of the present system.

Specific goals of the current upgrade effort include: 1) elimination of VCO frequency drift with time and temperature, 2) capability of switching between operational states on a machine cycle-by-cycle basis, 3) ability to synchronize a gap in the Booster beam to the extraction kicker for low loss, properly cogged transfer to the Main Ring, 4) built-in programmable flexibility, 5) enhancement of long term operational reliability and maintainability, and 6) improved remote diagnostic features.

III. STATUS

Replacement of the analog VCO frequency source with a more stable and precisely controllable source is key to the merit and success of any upgrade of the Booster LLRF. The feasibility of using a DDS operating directly at the Booster frequency to accelerate beam was demonstrated more than two years ago by Mestha et al.[5,6] In February of this year, the DDS used for that demonstration was revived, coupled with a new digital signal processor, and made to accelerate beam in the Booster once again. This proof-of-principle DSP/DDS frequency source has now been used to operate the Booster for short periods while running for antiproton production. Its use other than for limited periods under closely monitored conditions is precluded, not by performance limitations, rather by lack of suitable interfacing to the Fermilab accelerator

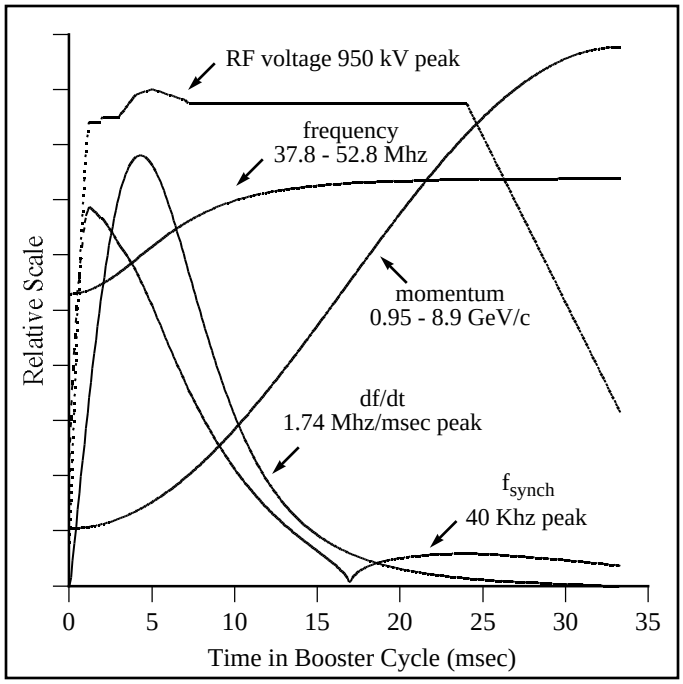

Figure 1: Selected Booster Parameters.

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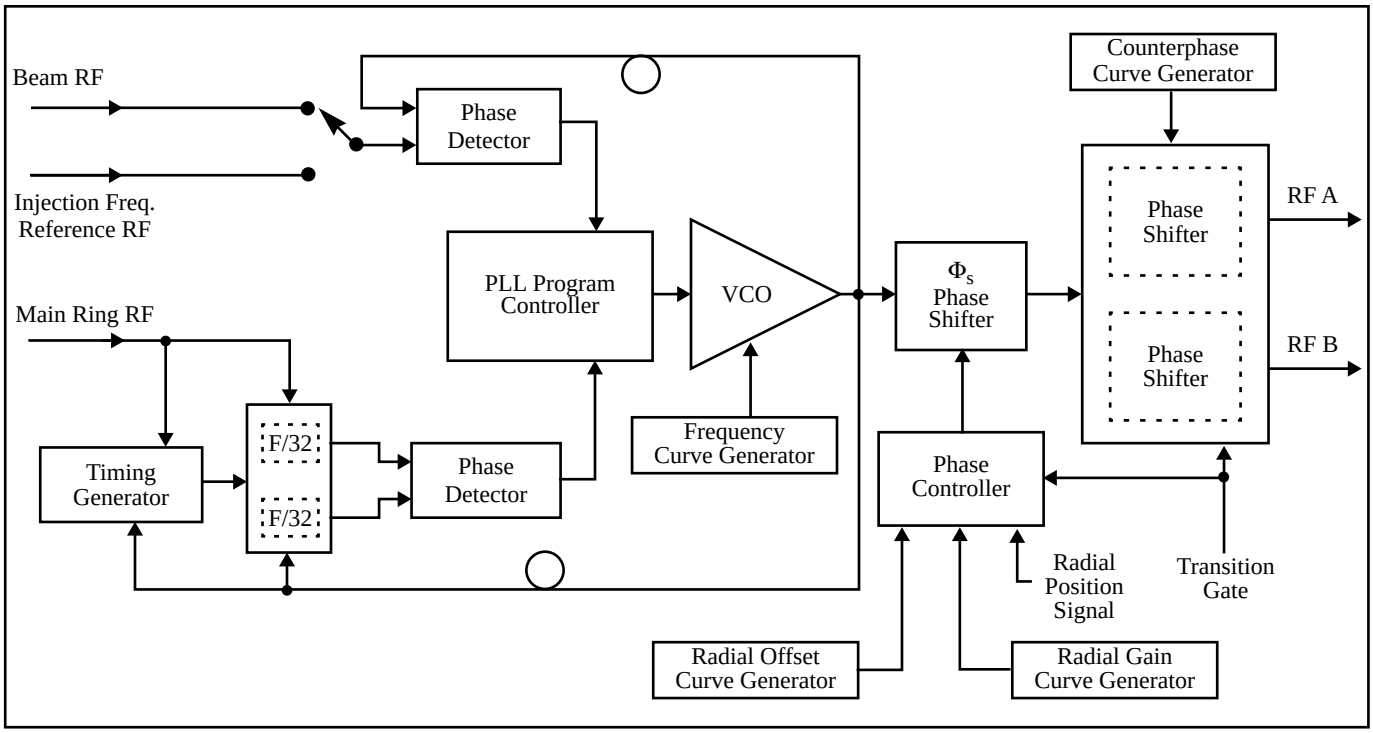

Figure 2: Booster LLRF Block Diagram

control system network (ACNET).

The prototype DSP/DDS frequency source is designed to function within the present LLRF system by simply substituting for the analog VCO and the CAMAC frequency curve generator. Since the LLRF system provides damping of coherent beam phase oscillations by operating the VCO in a beam-referenced phase-locked loop configuration, the DSP/DDS combination is required to meet all performance criteria necessary to stably fulfill that function. The crucial parameters are loop bandwidth and signal transport delay. Given the maximum synchrotron frequency of 40 Khz (Fig. 1), a real-time loop bandwidth of several times that is required, implying correspondingly short signal transport delay times.

As shown in Figure 3, the prototype source is comprised of an Analog Devices ADSP-21020 DSP, a Stanford Telecom STEL-2273A DDS, and two high speed analog to digital convertors (ADCs). A DOS-based computer hosts the software development and program downloading tools. The DSP is used directly as provided on the ADSP 21020 EZ-LAB Evaluation Board. It runs with a clock speed of 25 Mhz. This DSP was available as a result of concurrent Main Ring and Tevatron LLRF improvement efforts utilizing this DSP family. The 2273A DDS is a board level product based on Stanford Telecom's STEL-2173 GaAs numerically controlled oscillator chip. It was selected for this application after DDS products from another manufacturer were tested and observed to exhibit unacceptable phase discontinuities when programmed through certain frequency transitions. Though specified up to 1 Ghz, the DDS is operated with a 576 Mhz clock to minimize the need for high order control bit manipulation and to avoid certain close-in spurious frequency conditions within the Booster frequency range. The output from the 2273A is used directly with no additional filtering except as provided by the *Q* of the accelerating cavities. Spurious frequencies as large as -45 dBc are observed out of the DDS, but present no apparent problem to the Booster beam. Presumably the fast frequency sweep prevents any one 'bad' spur from persisting long enough to cause beam blow-up. The ADCs are Analog Devices part AD773 which operates with a 5 cycle pipeline delay. To minimize their contribution to signal transport delay, they are clocked at the full rated speed of 10 Mhz. One ADC processes the fast phase detector signal required for phase-locking operations. Its data is read by the DSP once per microsecond while phase-locking to the beam for acceleration or to a Main Ring rf signal for extraction synchronization. The other ADC is read only once each 15 Hz Booster cycle to provide operator control of the frequency at injection.

An interrupt driven program runs on the DSP to write an

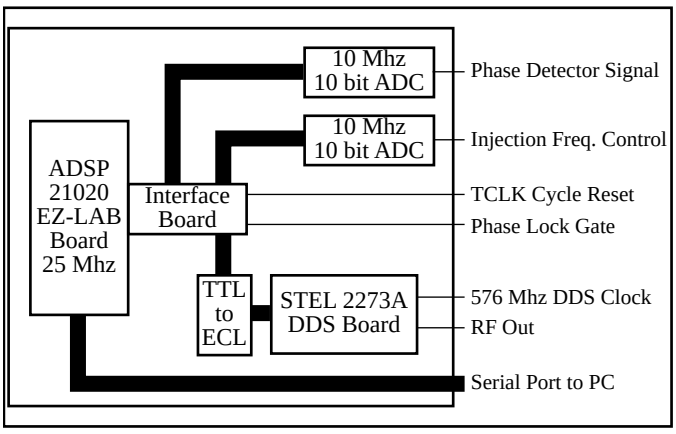

Figure 3: DDS/DSP Prototype Block Diagram

updated frequency setting to the DDS once per microsecond. The Fermilab timing system provides a 15 Hz interrupt to synchronize the frequency sweep to the Booster cycle. Within each cycle, the 21020's internal timer is used to generate regular interrupts every 2 μsec. A fast interrupt service routine is thereby invoked to step through the pre-calculated frequency table residing in DSP memory and, at two times separated by 1 μsec, to read and process the digitized phase detector information (for once per microsecond feedback.) Eleven DSP cycles (about 440 nsec) are required to read the ADC, process the information, and write a new setting to the DDS. Including the 0.5 μsec ADC pipeline, the total feedback signal transport delay from phase detector to change in DDS output frequency is then < 1 μsec.

Operating in this manner the DSP/DDS frequency source is able to support a stable phase-locked loop closed loop bandwidth exceeding 150 Khz. Within the framework of the existing LLRF system, it has successfully accelerated beam in the Booster during normal high intensity operations. Acceleration efficiency comparable to that of the analog system was achieved with little fine tuning.

IV. PLANNED SCOPE OF THE UPGRADE

The block architecture of the present system is planned to be maintained as the core of the upgrade. All the existing CAMAC LLRF curve generators and NIM housed RF circuits will be replaced with new hardware built in VXI format. A National Instruments CPU030 running VXWorks will serve as the crate Slot 0 controller and provide the interface to ACNET.

Figure 4 depicts the planned crate layout and individual board functions (compare to Fig. 2). The frequency source DSP provides the Frequency curve generator functionality. A second DSP, on the Phase Controller board, serves the roles of the present Radial Offset, Radial Gain, and Counterphase curve generators. In addition, it is expected that this DSP, perhaps in communication with the other, will provide the horsepower to implement a ‘trip plan’ type synchronization scheme, as described by Mestha [7], for extraction to Main Ring. The ability to time a gap in the Booster beam to the extraction kicker firing is considered extremely important to minimize radiation from beam loss during future high intensity, high repetition rate Booster operation.

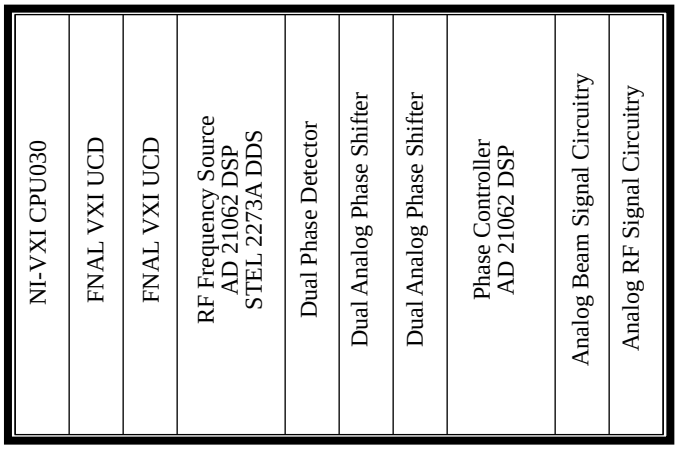

Figure 4: Conceptual Layout of Booster LLRF VXI Crate

V. SUMMARY

The proof of principle of using a DDS directly as a frequency source for the Booster has been solidly established. This offers, for the first time in that machine, an opportunity to explore the many benefits that a stable and precise frequency source may provide. A plan has been laid out to design and fabricate the necessary hardware and control system interface required to take full advantage of this opportunity. Much of the new system is expected to be operational by the end of this calendar year. Meanwhile, the prototype remains available for operation within the existing Booster LLRF.

VI. ACKNOWLEDGMENTS

Steve Bjerklie has designed, assembled, and tested the hardware used in the successful prototype. Keith Meisner and Brian Chase, working on the Main Ring and Tevatron LLRF system, have laid much groundwork for this effort and provided valuable guidance in application of the DSP. Acknowledgment is also made of work done by L.K. Mestha, Victor Brouk, Tom Uher et al. at the SSC which forms the basis for the current approach to beam transfer synchronization.

VII. REFERENCES

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