Digital I/Q Demodulator*

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Abstract

I/Q demodulation is a common and useful RF signal processing technique used in charged-particle accelerators. When implemented with conventional analog RF components, a number of inherent errors can degrade the I/Q Demodulator performance, including gain balance, quadrature-phase balance, DC offsets, impedance match, and carrier leakage. Recent advances in high-speed analog-to-digital converters allow the I/Q demodulator to be implemented digitally, greatly reducing these systematic errors. This paper describes the design of a digital I/Q demodulator that will be applied to the PEP-II B factory.

1. INTRODUCTION

The PEP-II B factory has a number of RF feedback control loops and algorithms that collectively maintain the proper RF field conditions for acceleration and damping of the longitudinal coupled-bunch beam instabilities [1-3]. The setup and operation of the control loops require a method of making very accurate RF measurements of the various signals throughout the RF system for the PEP-II accelerator. These measurements directly affect the operational stability and control for the PEP-II RF system, and thus, must be very precise and time-invariant. It is desired to measure the RF signals with accuracies of $0.1°$ in phase and 0.1% in amplitude over a dynamic range of approximately 30dB. Resolving the RF amplitude and phase information into their in-phase and quadrature (I/Q) components during demodulation is advantageous because of the symmetry of the I/Q signals and the less-complicated nature of the I/Q electronics. Precision RF measurements for PEP-II shall be accomplished with a digital I/Q demodulator employing a quadrature IF sampling technique.

2. THEORY

The conventional analog I/Q demodulator, shown in figure 1, uses two matched demodulator circuits to convert the RF input signal directly to baseband analog I and Q signals that are subsequently converted to digital data. The functionality of this circuit is based upon the RF input signal being split and mixed with two local oscillator (LO) signals that have a $90°$ phase shift between them. This $90°$ phase shift provides the mechanism to distinguish the I and Q components of the RF signal. The mixer outputs are lowpass filtered to remove the high-frequency mixing products, providing baseband analog I and Q signals that are sampled and converted to digital values. The parallel nature of the analog I/Q demodulator requires the two legs to be very closely matched to each other for accurate I/Q measurements. Also, the quadrature phase shift must be exactly $90°$ at all frequencies. This nature of the conventional analog I/Q detector makes it susceptible to errors associated with gain matching, DC offsets, quadrature phase errors, carrier leakage, and impedance matching. These errors can be difficult to completely eliminate or compensate for, causing RF measurement errors.

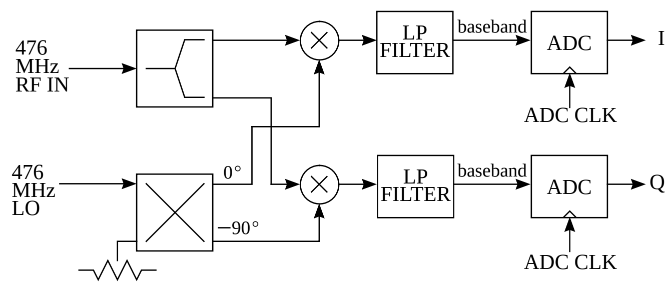

Fig. 1. Conventional Analog I/Q Demodulator.

As an alternative to the analog I/Q demodulator, figure 2 shows a digital I/Q demodulator implementation that inherently improves performance. Within this implementation, the RF input is downconverted to an IF of 4.9 MHz by mixing the RF with a 471.1 MHz LO. The resulting signal is bandpass filtered to remove the high-frequency component that results from mixing and also limit the signal bandwidth to avoid aliasing. Aliasing is discussed in detail in a following section of this paper. The 4.9 MHz IF output is directly sampled with an analog-to-digital converter (ADC) operating at 19.6 MSPS. The time period between consecutive ADC samples is 50.95 ns which corresponds to exactly $90°$ at the 4.9 MHz IF. The sampled data reflects the amplitude of the original RF signal sampled at $90°$ intervals. If we define the first sample at $0°$ as I, the next sample at $90°$ is Q, the following sample at $180°$ is -I, the next sample at $270°$ is -Q, the following sample at $360°$ is again I, and so on. The ADC output provides a data stream consisting of the repeating pattern of measurements of I, Q, -I, and -Q. The I and Q variables within this digital data stream are separated by a multiplexer that switches every other sample into two parallel digital paths. The sign inversion in each path is removed by multiplying each data stream by +1 and -1 alternately. The resulting outputs correspond to the measured I and Q of the input RF signal.

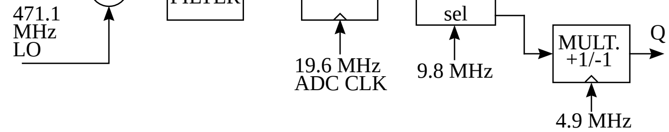

Fig. 2. Digital I/Q Demodulator.

The advantages of the digital I/Q demodulator are significant. The single path for the RF and IF processing insures per-

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fect gain-matching between the two I and Q signals. The two paths are applied to separate circuitry only after they have been converted to digital data. All digital processing can be easily matched for the two signals. The concerns of gain balancing and impedance matching for all the RF and analog components is obviated. Also, because the IF signal is sampled without ever being downconverted to baseband, DC signals are not measured by the demodulator. Consequently, analog DC offsets and drifts do not affect the digital I/Q demodulator. The quadrature phase shift is dependent upon the precise timing of the ADC. The aperture jitter of the selected ADC is inconsequential, and stable clock circuitry have been designed into the PEP-II low level RF (LLRF) system. The one source of error for the digital I/Q demodulator results from the nature of the sampling process. The ADC clock period of 50.95 ns provides an exact $90°$ phase shift at the center frequency only. Signal frequencies not equal to the center frequency contain a quadrature phase error when measured. For a limited signal bandwidth, this quadrature phase error is maintained at insignificant levels, well below that achievable by conventional means. Narrow-band signals within 5 kHz of the RF carrier are detected with better than $0.05°$ quadrature error. Signals within the detection bandwidth of the I/Q demodulator (± 50kHz) are detected with better than $0.5°$ quadrature error.

3. IMPLEMENTATION

PEP-II requires approximately 20 precision I/Q measurements for each of the eight RF stations. In addition to the I/Q measurements, the amplitudes must be detected for those same 20 RF signals. Consequently an 8-channel I/Q & Amplitude Detector has been designed for PEP-II. The VXIbus form-factor has been chosen for the LLRF system because of the extensive computational requirements. The 8-channel I/Q & Amplitude Detector has been designed as a single-wide C-size VXIbus module. This module includes eight digital I/Q demodulators, eight RF amplitude detectors, extensive digital signal processing circuitry, and the VXIbus interface electronics.

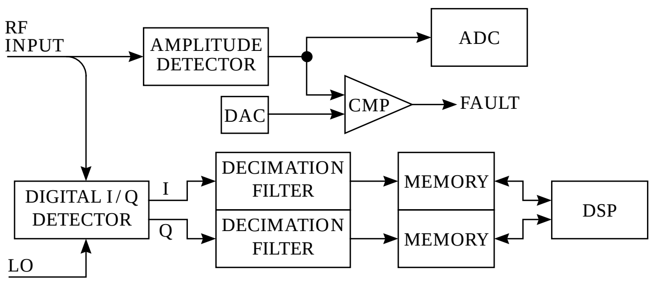

Fig. 3. One Channel of I/Q & Amplitude Detector.

Figure 3 shows a block diagram of one channel of the I/Q & Amplitude Detector module. The RF input, at a level of approximately 1 Watt (+30dBm) is processed in two separate circuits. The majority of the signal power is fed into an RF amplitude detector consisting of a forward-biased rectifying diode. A second matched diode is used to offset the forward bias voltage of the detection diode. This amplitude detector provides about 50 dB of measurement dynamic range and 30 dB of linear dynamic range for amplitude detection. The output is converted to a digital value for diagnostics and also compared to a fault threshold to indicate overload conditions. A small portion (approximately 1 mW) of the input signal is coupled into the digital I/Q demodulator described earlier. The digital I and Q outputs are processed in digital decimation filters that provide filtering to reduce the data rates from 755 kHz down to as low as 25 Hz. It is significant to note that the data is truly filtered from input bandwidths of a few MHz to output bandwidths as low as 1 Hz in order to avoid any aliasing of the measured data. The data is stored in a history buffer that can be used to display waveforms versus time, or for additional processing with an on-board digital signal processor (DSP). The DSP provides the capability of sophisticated on-board computation, such as converting I and Q to amplitude and phase, performing additional filtering and decimation, and processing data through control algorithms. The net result is a very flexible and powerful instrument for RF signal processing.

The ADC used for direct digital sampling of the IF signal must provide an input bandwidth much greater than the IF frequency (4.9 MHz) and must operate at the required sampling rate of 19.6 MSPS with a vertical resolution of 12 bits. The Comlinear Corporation CLC949, a 12-bit, 20 MSPS ADC, has been selected for the direct I/Q sampling. In order to reduce size and cost of the I/Q demodulator circuitry, a single ADC is used to sample the eight separate IF signals. Figure 4 shows a block diagram of the multiplexing scheme used to process eight IF signals with a single ADC. This multiplexing scheme provides a significant cost savings because the high-performance ADC is a very costly item.

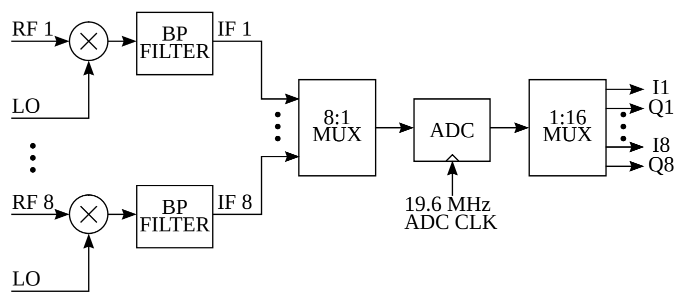

Fig. 4. Applying one ADC to eight I/Q channels.

There is a trade-off associated with using a multiplexer for the eight I/Q demodulators. Without the multiplexer, each channel is sampled at the full 19.6 MSPS, providing unaliased I/Q data with a maximum single-sided bandwidth (SSBW) of approximately 9.7 MHz. Figure 5 shows a graph of the time response of the multiplexed I/Q sampling technique. After sampling a channel twice at the 19.6 MSPS ADC sampling rate, the IF multiplexer is switched to the next channel, which, after allowing the IF signal to settle, is sampled twice also. After cycling through all eight channels, the multiplexer waits an additional 101.9 ns before sampling the first channel again. These extra two clock cycles provide the $180°$ phase shift to rotate the IF phase to correspond to -I and -Q. The sign inversion, which is necessary to insure insensitivity to analog DC offsets, is removed by the digital +1/-1 multiplier. The resulting time period between consecutive samples for one channel is 1.325 µs, corresponding to a sample rate of 755 kSPS. This defines the bandwidth for the bandpass filter that is applied to the IF signal to avoid aliasing during sampling.

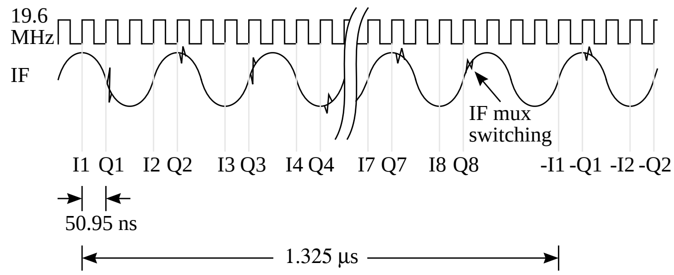

Fig. 5. Time response of I/Q sampling.

Figure 6 shows the frequency response of the I/Q sampling technique. The top graph shows the spectrum of a single IF channel after being mixed with the LO. Note that in order to avoid aliasing in the downconversion process, the SSBW of the RF input must be less than 9.7 MHz. The IF signal is first processed in a narrow-band bandpass filter and then sampled by the ADC. Sampling the IF signal at the 755 kHz sample rate reproduces the filtered IF spectrum at 755 kHz intervals as shown in the middle graph. This indicates that in order to avoid aliasing within the I/Q Demodulator's detection bandwidth of ±50kHz, the bandpass filter must limit the SSBW of the IF signal to less than 700 kHz. The bottom plot shows the signal spectrum after being processed by the digital +1/-1 multiplier. Multiplication by a repeating pattern of +1 and -1 is comparable to mixing the sampled IF signal with a sampled 377.5 kHz sinusoid, which provides a frequency shift of 377.5 kHz. Because this final frequency shift down to baseband is performed digitally, the data does not contain any errors associated with analog DC offsets. Due to the precise nature of digital electronics, all subsequent digital processing does not introduce any errors into the signal data either.

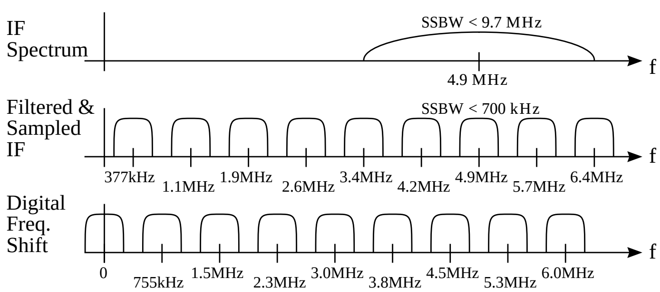

Fig. 6. Frequency response of I/Q sampling.

The dynamic range of the I/Q demodulator is approximately 60dB. The upper limit is determined by the distortion and compression caused by the downconversion mixer at high RF input power levels. In order to maximize this upper limit, a high-level mixer requiring a +17 dBm LO is used. By defining the maximum RF input to be 0 dBm, the distortion due to intermodulation products and gain compression is kept below 0.1%. The high-level mixer also maintains a constant insertion phase for RF inputs below 0 dBm. The lower limit of the dynamic range for the I/Q demodulator is determined by the thermal noise. The noise introduced by the RF circuit is insignificant because its noise bandwidth is limited by the narrow-band anti-aliasing filter. Noise is introduced by the IF buffers, the IF multiplexer, and the ADC. For the I/Q demodulator, the signal-to-noise ratio has been computed to be better than 65dB.

4. MECHANICAL DESIGN

The mechanical design for the I/Q & Amplitude Detector module is not trivial. The dimensions of a C-size VXIbus module severely limit the physical size of the electronics. In order to maintain adequate shielding and a temperature-controlled environment for the analog (RF/IF) circuitry, an ovenized RF enclosure is required. Surface mount technology is used for the entire analog circuit within the enclosure. This circuit is implemented as a microstrip printed-circuit board (PCB). Figure 7 shows the CAD layout for a single channel of the I/Q & Amplitude Detector electronics. With no through-hole components, the PCB is mounted directly to the bottom of the RF enclosure, providing good thermal and electrical contact. The whole enclosed circuit is heated and regulated at 60°C, which is above the maximum ambient temperature. The constant temperature for the analog electronics maintains constant insertion losses, insertion phases, and return losses for the various components.

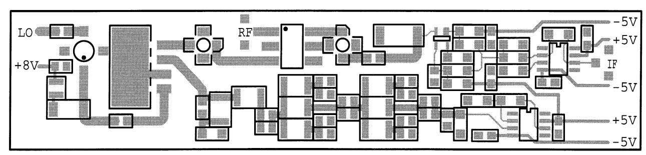

Fig. 7. Microstip layout of I/Q & Amplitude Detector channel

5. SUMMARY

The I/Q & Amplitude Detector module is a sophisticated electronic instrument that makes use of novel ideas and technology to enable powerful RF measurements and signal processing. The high density of channels per slot and integrated processing power reduce the overhead costs for the PEP-II LLRF system. The performance specifications for the I/Q & Amplitude Detector module can be summarized as follows:

- I/Q Demodulator Dynamic Range: 60 dB
- I/Q Demodulator Accuracy: ±0.1%
- I/Q Demodulator Phase Stability: ±0.1°
- I/Q Demodulator Detection Bandwidth: ±50kHz
- Amplitude Detector Dynamic Range: 50 dB
- Amplitude Detector Linear Range: 30 dB
- Amplitude Detector Accuracy: ±1%
- Amplitude Detector Detection Bandwidth: ±5MHz

6. REFERENCES

[1] P. Corredoura et. al. "Low Level RF System Design for the PEP-II B Factory", this conference (PAC 95).
[2] P. Corredoura, L. Sapozhnikov, R. Tighe, "RF Feedback Development for the PEP-II B Factory" Proceedings of the 1994 European Particle Accelerator Conference.
[3] P. Corredoura "Development of Digital Control for the PEP-II Klystrons" SLAC PEP-II Tech Note #60, 1994.