SINGLE-TURN BEAM POSITION MONITOR FOR THE NSLS VUV ELECTRON STORAGE RING *

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Abstract

A "fast" beam position monitor capable of measuring the position of a circulating bunch in the VUV electron storage ring is presently under development. This monitor will collect data at a rate of about 6 x 10^6 measurements/sec per channel. We describe the design and operation of the monitor and the processing of the acquired data.

I. INTRODUCTION

The NSLS VUV electron storage ring typically operates at 800 Mev with a peak stored current of approximately 800 mA. In the ring, electrons may be stored in any pattern consisting of up to nine bunches (harmonic number h=9). The position of the beam orbit is continuously monitored at 24 locations around the ring circumference with dedicated high resolution beam position monitors (RFBPMs) which process rf signals derived from button pick-up electrodes (PUEs) embedded in the machine vacuum chamber wall [1]. These RFBPMs measure beam motion in the frequency range from DC to about 2 kHz, so that their output represents an average position of the beam at the PUEs over many revolutions around the ring.

Since many important phenomena occur at or near the beam revolution frequency, which in the case of the VUV Ring is approximately 5.9 MHz, a single-turn beam position monitor (STBPM) capable of making a position measurement during a single passage of a bunch past a pick-up electrode station or during many successive passages of the same bunch is now under development. In the VUV Ring, STBPMs will be used to study (a). closed orbit fluctuations, (b). correlation between orbit fluctuations, (c). growth and damping rates of transverse instabilities, etc., as well as in the optimization of injection system parameters during routine operations.

The “fast” monitor will process sub-nanosecond wide bipolar PUE pulses with a wideband hybrid network to form sum and difference signals. These signals will be synchronously detected, integrated and then digitized with a very fast A to D converter. Beam position will be calculated by dividing the difference by the sum digitally. Due to the high revolution frequency, data will be collected during the approximately 180 nsec long revolution period on one bunch only. To reduce errors in the data due to additive circuit noise, the output of the integrator will be sampled twice during each period (the second time when there is no signal) and the readings will be subtracted. The “fast” monitor will share the rf signals from the PUEs with the “slow” BPM. We describe the design and operation of the new monitor.

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II. PUE SIGNAL PROCESSING

The voltage signal from a ring PUE for a single bunch (14 mA, shortest bunch length σ_t=162 psec) circulating in the VUV ring acquired by a real-time oscilloscope is shown in Fig. 1a. The Fourier transform of this waveform in Fig. 1b demonstrates the high frequency response of these electrodes and shows that the spectral content of this signal lies in the range between a few tens MHz and 2 GHz. When the frequency data is corrected for the current distribution within the bunch, the resulting coupling impedance has a peak at about 900 MHz and a zero at 2.5 GHz.

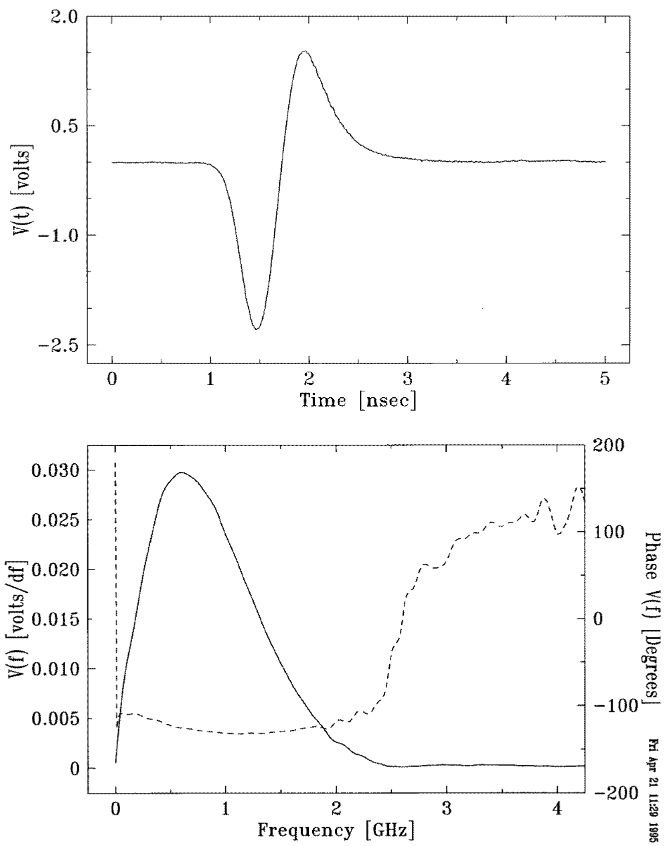

Fig. 1 A PUE signal (a) and its Fourier transform (b)

In order to process a set of four PUE signals and maintain stable gains and offsets, the differencing will be performed directly on the signals, i.e. prior to any amplification, using 180 degree wideband rf hybrids [2]. The present plan is to add directional couplers to the existing broadband signal cables and to provide 10 dB attenuated octave bandwith signals

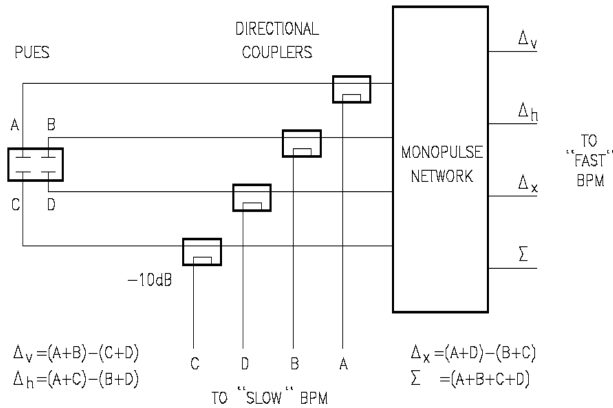

Fig.2 Fast analog signal processing

centered on 158.66 MHz to the RFBPM while making the broadband signals available to the STBPM. This coupling network and four-way hybrid are shown in Fig. 2. All cables between the PUEs, directional couplers and the hybrid must be carefully matched.

III. STBPM DESIGN

A. Processing Electronics

The front end of the STBPM consists of two channels which simultaneously process the difference and the sum signals from the hybrid network. Each signal is first stretched by a Gaussian filter from < 1 nsec wide to about 10 nsec. The stretched bipolar pulses are synchronously detected, i.e. rectified by a double balanced mixer whose LO input is derived from the sum signal as shown in Fig.3. The sum signal is processed by several stages of hard limiting before being used as the LO mixer input. The monopolar mixer output is integrated by a fast integrator whose output is sampled by a track and hold (T/H) amplifier. The integarator is reset after the T/H acquires its output signal level and remains in a reset state until just prior to the start of the next integration period.

In the front end electronics section, some noise is injected into the signal path by the mixer as well as by the integrator reset circuit. This additive noise can be removed from the output by sampling in between signal pulses to yield a noise signal measurement.

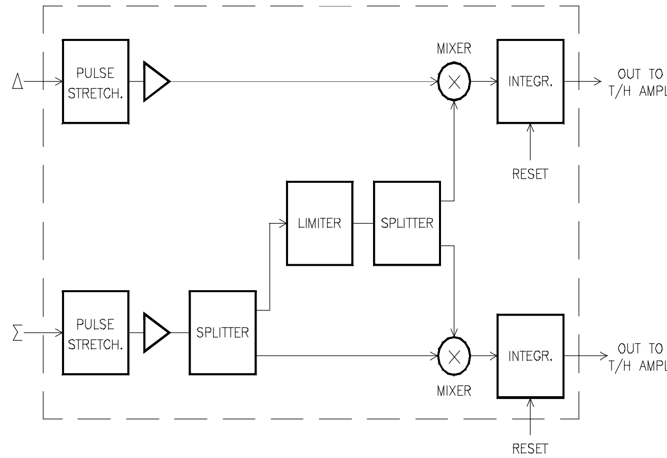

Fig. 3 BPM analog section

B. Analog to Digital Conversion

In each signal channel, the track and hold amplifier (Acculin AL-1210JR) acquires the integrator output signal in less than 10 nsec. This signal level is held by the T/H until it is processed by the 12-bit A/D converter (Datel ADS-119). The A/D output data is ready in less than 80 nsec after the start of conversion. After the completion of the A to D conversion cycle, the data is transferred to a FIFO buffer memory (32 K points/channel). The FIFO is interfaced to a PC-486 processor operating in a VXI environment via VME bus interface.

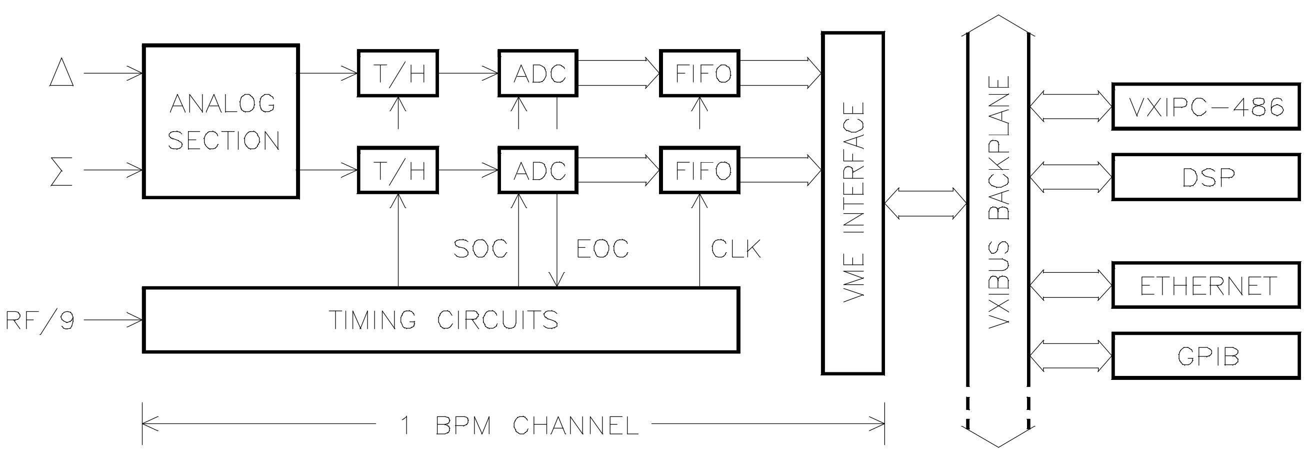

Fig. 4 Block diagram

C. BPM Operation

To desribe the basic mode of the monitor operation, we will refer to the block diagram in Fig. 4 and the timing diagram in Fig. 5. In Fig. 4, the Rf/9 input is the master trigger derived from the ring accelerating system 52.88 MHz drive signal. This trigger occurs once every bunch revolution period and is synchronized with the circulating bunch. The integrator reset input, the T/H control signals and the start of conversion pulse (SOC) are derived from the Rf/9 trigger and are appropriately delayed.

At the beginning of a revolution period, as the difference and the sum signals arrive at the inputs of the analog section, the integrator is ready to accept an input. The sum signal is constant in phase whereas the phase of the difference signal depends on the position of the beam relative to the electrical center of the PUEs. Both inputs are equally stretched and synchronously detected as described earlier. The above process detects the phase of the input signal so that the polarity of the sum signal will, for example, always be positive while that of the difference signal may be positive or negative.

Each of the detected signals is integrated and the result is sampled by the T/H and then digitized. To reduce errors in the readings introduced by switching noise in the electronics, the integrator is reset and sampled a second time approximately half-way through the cycle when there is no signal. The second reading is subtracted from the first after digitization. Also, since the difference signals are beam intensity dependent, they must be normalized by dividing by the sum signal which, of course, is also dependent on the intensity.

The above sequence will be started and repeated for as many cycles as commanded by the PC up to maximum available space in the FIFO buffer. The mixer operation is self-correcting for variations in the time of arrival of the input signals and the precision of all other timing signals is not critical in the operation of the monitor.

D. Data Processing

After accumulating a record of data in the FIFO buffer, the microprocessor will read the data, subtract the non-signal noise measurement point from the adjacent signal data point, normalize the difference value with respect to the simultaneously measured sum signal, and then convert these ratios to vertical, horizontal and quadrupole moment values for the bunch, respectively. Each buffer of bunch position measurements will be divided into sub-records of 1K or more data points and processed by the DSP using its built-in FFT processor. (≈20 msec. per 1K point FFT). The output will include an average value (closed orbit position) and several spectral peaks. Well defined signals from the betatron oscillations will be tracked as a function of time to determine their growth and damping rates and the effect of these amplitudes on averaged beam properties. Data obtained via the Ethernet on variation of other system parameters will be used to determine their impact on the amplitudes of these oscillations. Data from the closed orbit micro (from the RFBPMs) will be used to cross-calibrate the average value and to look for slower fluctuations of the closed orbit.

During machine studies periods, a fast bunch kicker will drive the transverse oscillations for linear and non-linear tune measurements and damping rates as a function of systerm parameters (e.g. chromaticity and sextupole strength). As more STBM channels are installed, the data from PUEs at different azimuthal locations around the ring will be analyzed for simultaneous readings of the closest bunch. This will yield important information on the modal structure of transverse oscillations [3]. If well defined modes are observed, they will allow the source of beam impedance that drives the transverse coupled bunch motion to be more easily studied.

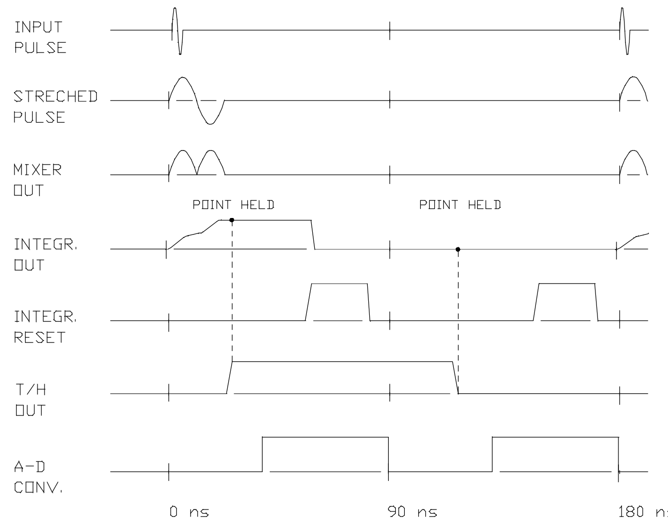

Fig. 5 Timing diagram

IV. REFERENCES

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