THE RHIC GENERAL PURPOSE MULTIPLEXED ANALOG TO DIGITAL CONVERTER SYSTEM*

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ABSTRACT

A general purpose multiplexed analog to digital converter system is currently under development to support acquisition of analog signals for the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory. The system consists of a custom intelligent VME based controller module (V113) and a 14-bit 64 channel multiplexed A/D converter module (V114). The design features two independent scan groups, where one scan group is capable of acquiring 64 channels at 60 Hz, concurrently with the second scan group acquiring data at an aggregate rate of up to 80 k samples/second. An interface to the RHIC serially encoded event line is used to synchronize acquisition. Data is stored in a circular static RAM buffer on the controller module, then transferred to a commercial VMEbus CPU board and higher level workstations for plotting, report generation, analysis and storage.

I. DATA ACQUISITION REQUIREMENTS FOR ACCELERATORS

The most unique requirement for a data acquisition system for accelerators is that sampling of data must be synchronized to accelerator system timing. At the workstation level, data acquired from multiple locations, must be time correlated for plotting and analysis. Another critical requirement for the RHIC system is to provide a historical data buffer, where all data is stored in a continuous circular buffer at a relatively slow acquisition rate (typically 60 Hz) until a critical event such as a beam abort occurs. Selected historical data may then be viewed for analysis, and to determine conditions that caused the critical event. While data is being stored in the historical data buffer, the system must be capable of concurrently scanning a few selected channels at a much faster sampling rate for a snapshot period of time.

II. BACKGROUND

Based on the above requirements and after researching commercially available hardware, it was determined that a custom hardware solution was necessary. Various design options and system architectures were considered, and the finalized design is discussed herein.

III. SYSTEM ARCHITECTURE

A block diagram of the overall system architecture is shown in figure 1, and the front panel layout for each module is shown in figure 2.

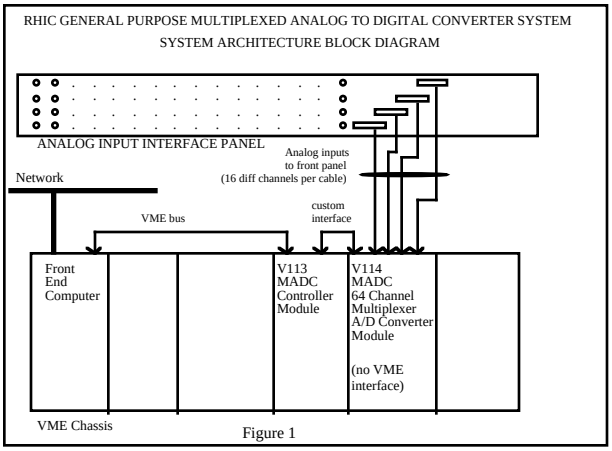

Figure 1

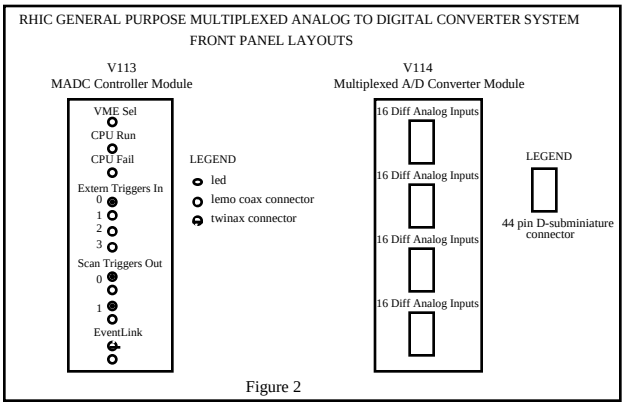

Figure 2

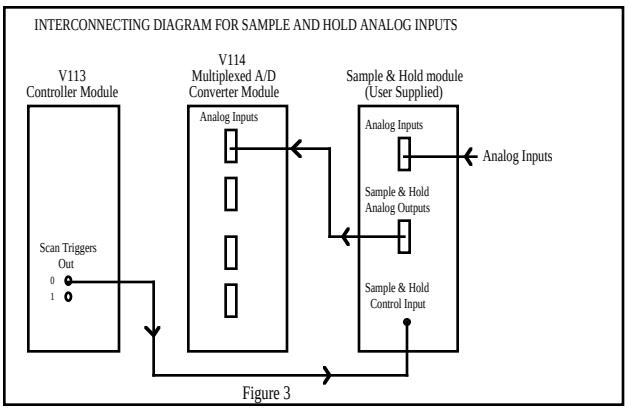

Figure 3

* Work performed under the auspices of the U.S. Dept. of Energy.

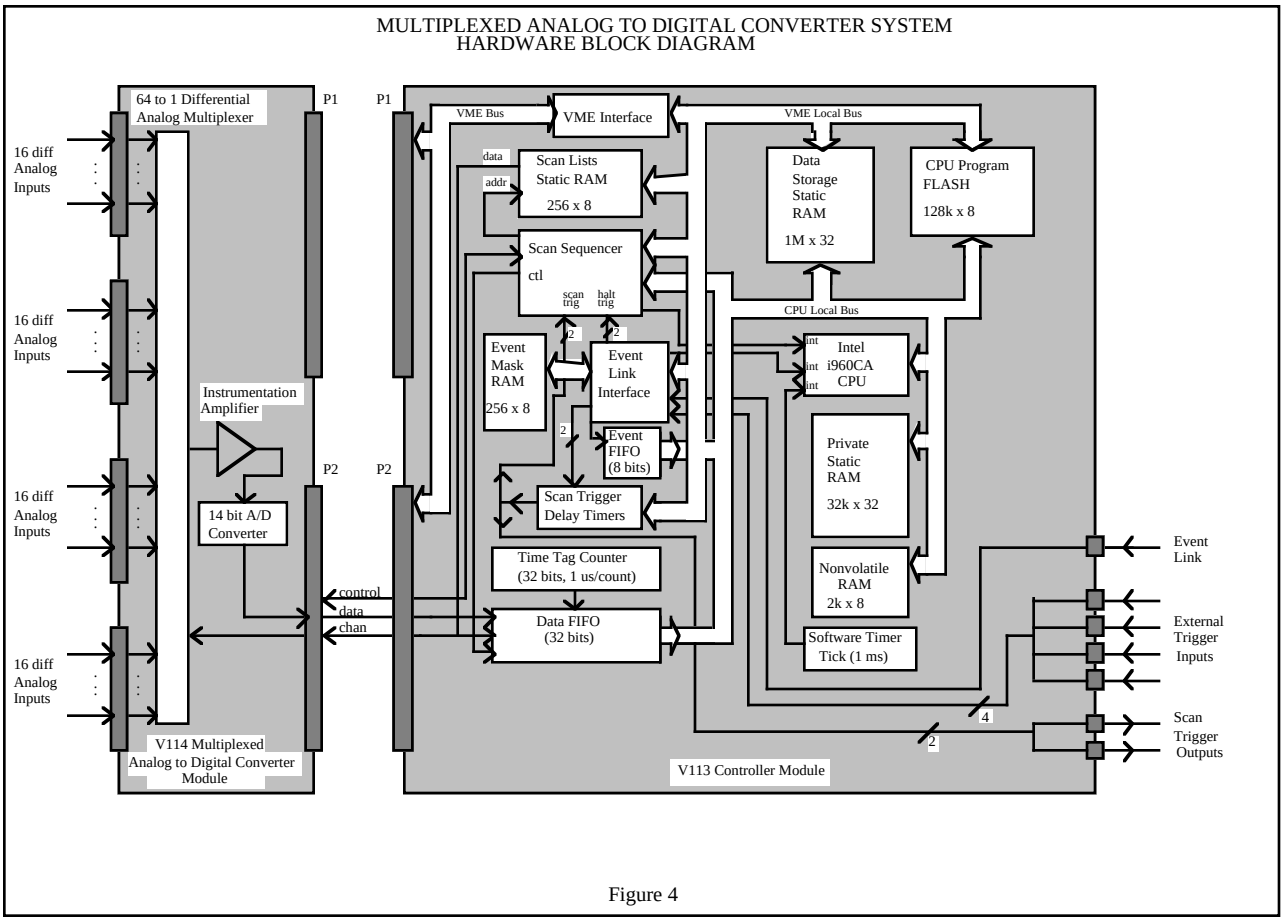

Figure 4

The RHIC multiplexed analog to digital converter system also provides the capability to be interfaced with a user supplied sample and hold module. The sample and hold analog outputs connect to the analog input connector on the V114 module. The sample and hold control is generated by the scan trigger output on the V113 module, as shown in figure 3.

A hardware block diagram for the V113 and V114 modules is provided in figure 4. The V113 controller module contains the VME bus interface, RHIC event link interface, data storage memory and all of the data acquisition system real-time intelligence. The V114 converter module contains the analog multiplexers, instrumentation amplifier, A/D converter, and a custom interface to the controller module through user defined pins on the VME bus P2 connector.

IV. SYSTEM FEATURES

A summary of the system's capabilities is detailed below.

A. Scan Groups

Two idendical scan groups are provided. Each scan group is configured with the following information.

a. Scan list containing all the channels to be scanned.
b. Arm trigger setup.
c. Halt trigger setup.
d. Scan trigger setup.

Typically scan group 0 will contain all defined analog inputs, and will be configured to continuously scan at a rate of 60 Hz for use as a history buffer. Data acquisition will be configured to halt on a specified system event for postmortem analysis of beam aborts. The front end computer reads this buffer to obtain the most recent data for each analog input.

Scan group 1 will normally be used to acquire data according to application specific channel selection and timing requirements.

The following parameters are programmable for each scan group.

Arm/halt trigger source
One source is used for both the arm and halt trigger. This is configurable to be one of the following.
a. Single event or logical OR of group of system events.
b. External trigger.

Scan trigger source
The scan trigger source is configurable to be one of the following.

a. Single event or logical OR of group of system events
b. External trigger.

Arm trigger setup
The arm trigger is defined as the condition that causes data samples to begin being stored in the data buffer. After the arm trigger occurs, data samples will be acquired and stored on every scan trigger until the halt trigger occurs. The arm trigger is configurable to be one of the following.

a. Arm immediately on start command from front end computer
b. Arm on arm/halt trigger source
c. Arm on ms delay after arm/halt trigger source

Scan trigger setup
The scan trigger is defined as the condition that causes a single acquisition of all channels in the scan group. Scan triggering will occur only when scanning is armed as defined by the arm trigger. The scan trigger is configurable to be one of the following.

a. Scan on every period of programmable on-board clock (μs resolution)
b. Scan on scan trigger source.
c. Scan on *n*th scan trigger source
d. Scan on programmable delay after scan trigger source (μs resolution)

Halt trigger setup
The halt trigger is defined as the occurrence of a condition that causes data acquisition to halt. After the halt trigger occurs, data acquistion will stop and an interrupt will be sent to the front end computer. The halt trigger is configurable to be one of the following.

a. Scan continuously until front end computer commands stop
b. Halt when data buffer full
c. Halt on arm/halt trigger source
d. Halt on ms delay after arm/halt trigger source
e. Halt on number of scans after arm/halt trigger source

Reset at end of scan
Each scan group may be configured to reset the arm/halt trigger and the scan enable at the end of each complete scan.

B. On-board Data Buffer Memory

Data buffer memory is typically divided into two buffers, one for the scan group 0 and one for the scan group 1. The data buffer size is programmable in number of full scans. A full scan consists of one reading for each channel in the scan group. Data will be stored in a circular fashion, where the oldest data is overwritten as new data is acquired.

The V113 module may be populated with 1, 2, 3, or 4 Mbytes of data storage memory. The entire data storage memory is mapped to VME A32 space on a switch selectable 4 Mbyte boundary (A31..A22). VME data transfers supported include D32, D16, D08(EO), and BLT (block mode transfer).

Event mask RAM (256 bytes), scan list RAM (256 bytes), program FLASH (128 Kbytes), and configuration registers are mapped to VME A24 space on a switch selectable 256 Kbyte boundary (A23..A18). VME data transfers supported for this area are D08(EO) only.

C. Maximum Scan Rates

Maximum scan rates supported are as follows:

64 chans at 60 Hz for one scan group simultaneously with an aggregate rate of 80 KHz for the second scan group (1chan at 80 KHz, 2 chans at 40 KHz, etc).

Maximum continuous throughput from the V113 controller module to the front end computer, then to the higher level workstation is dependent on the network bandwidth. The goal is to provide a continuous update of 6 channels at 720 Hz to the requesting workstation. This translates to a network bandwidth requirement of:

720 scans/sec * 6 samples/scan * 2 bytes/sample
= 8640 bytes/sec

Faster acquisition will be provided with a snapshot mode, where the data acquisition is halted while the front end computer passes data to the higher level workstation.

V. ACKNOWLEDGEMENTS

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