

ACCELERATOR TIMING AT BROOKHAVEN NATIONAL LABORATORY*

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Abstract

Accelerator timing at Brookhaven National Laboratory has evolved from multiple co-axial cables transmitting individual pulses in the original Alternating Gradient Synchrotron (AGS) design, to serial coded transmission as the AGS Booster was added. With the implementation of this technology, the Super Cycle Generator (SCG) which synchronizes the AGS, Booster, LINAC, and Tandem accelerators was introduced. This paper will describe the timing system being developed for the Relativistic Heavy Ion Collider (RHIC).

I. INTRODUCTION

A modern accelerator must synchronize the operations of equipment over a wide area. In the early days of the AGS, the timing system consisted of a group of master clocks which generated clock trains, and a few key timing pulses. The clock trains were resynchronized to the start of each main magnet cycle. Clocks were distributed to equipment locations on individual co-axial cables using 16 to 20 V transformer isolated pulses known as an AGS standard pulse. This signal level was chosen to guarantee the signal would be reliably detected in electrically noisy environments

Delays necessary for sequencing systems were created using counters that counted down using one of the master clock trains. Timing triggers required in multiple locations were distributed from location to location using the same co-axial cable and AGS standard pulses.

The drawback of this system was the large number of cables to the many equipment locations. Another was the energy of the AGS pulse level. Low level analog and

digital circuits suffered from the ground bounce at the receiver.

II. AGS Booster

With the design of the Booster, additional requirements were imposed on the timing and control system. Pulse to Pulse Modulation (a term originally used at CERN) is an operating mode which permits changing the setup of the accelerator from cycle to cycle. To accomplish this, a Super Cycle Generator was designed to schedule the LINAC, Booster, AGS and Tandem Van de Graff. Multiple "users" are defined for each machine. Scheduling of active users is accomplished via timing signals initiated by the central timing system. Naturally, if each timing pulse was transmitted on a separate cable (there are currently 60 timing events identified for the Booster) the number of cables required to support Booster operations would be prohibitive.

The cabling issue was overcome by a system first developed at Fermilab. Pulses on individual cables were replaced with digital codes transmitted on a single serial link. This technique permits multiplexing of timing information on a single cable. The event codes are transmitted using a serial modified Manchester code (bi-phase mark). The transmission rate is 10 Mbits/sec, and 1.2 usec are required to transmit an event code. The event link transmits a continuous bi-phase-mark "ones" transmission during idle periods. A restriction of using a serial link is, since only one event can be transmitted at a time, they must be prioritized.

The Booster has used the serial timing distribution scheme since it was commissioned in 1989. Because of the rapid cycling nature of the Booster (7.5 Hz) the central timing generator for this

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accelerator is table driven. Multiple tables permit rapid switching of timing setups. Each table contains an ordered list of events to be broadcast and the times at which they must be transmitted. The basic resolution of the system is 1 μ s. Software precludes contention by scheduling events at least 2 μ s apart. One limitation of the present design is that no provision currently exists to generate single occurrences of events or generate events from external (hardware generated) timing pulses.

III. RHIC Collider

The RHIC collider, currently being designed and built, requires a slightly different timing approach. The RHIC cycle is expected to be up to 10 hours long. During collision mode, timing events are more likely to be of an asynchronous nature, which is not well suited to table driven scheduling. Timing events and clocks from this link will be used to initiate hardware operations including changes in settings, state changes, and data acquisitions. Events may also be required by software running on systems not directly coupled to accelerator hardware. A standard clock frequency of 10 MHz, as is presently used in the AGS and Booster, provides adequate resolution for timing events in the RHIC acceleration and collision processes.

Event sequences to initiate waveforms and acquire data during the acceleration cycle, tune measurements, etc., will be implemented by cascading programmable delays. Clocks that are of a general interest, such as the line locked 720 Hz clock, generated by the main magnet power supply system, will also be available on the RHIC event link. Externally generated events may also come from other systems sensing unusual conditions with the beam. In the case of a beam abort, the abort event can be utilized to freeze circular buffers in data acquisition systems for post-mortem analysis.

An example of a software generated event would be one to synchronously activate new settings after they have been

loaded and verified. Software generated events may also provide a convenient way to commission new systems.

The probability exists that event requests could occur overlapped in time. Since only one event can be processed at a time, priority resolution will be an integral part of the central encoding facility. Event contention is handled in hardware with highest priority given to input 0 and lowest given to input 255. It should be pointed out, however, that lower priority events being processed will not be interrupted by the arrival of a higher priority event request.

The RHIC central event encoder its input modules, and supporting host computer interface occupy a single 21 slot VME chassis. The event system interconnections are point-to-point, differential TTL, isolated at the receiving end by transformer coupling.

Interbuilding transmission to remote RHIC equipment locations is via single mode fiber optic transmitters and receivers.

At each RHIC equipment location, the optical transmission is converted back to electrical and buffered as differential TTL. A fanout/repeater is used to produce multiple outputs. General purpose decoder/delay modules may be located in these remote locations, as well as other specially designed modules having direct event link inputs (e.g., the waveform generator).

RHIC event codes can be permanently assigned without regard to their event link transmission priority level. This allows an event code trigger priority level to be adjusted relative to other event codes without changing the event code.

EVENT ENCODER MODULE

The event encoder module provides event code translation, computes the parity and encodes the event into a bi phase mark serial data stream for transmission on the RHIC timeline. As the code is serialized, a "zero" start bit is added, and code parity (even) is generated. The

output of the bi-phase-mark converter is transmitted over the RHIC event link.

The encoder module is connected to a 16-position event input module bus. At the end of the event code transmission, the encoder allows the event input module priority system time to determine the next event trigger (if any) to be transmitted by the encoder module, and maintain minimum headway. The event trigger with the lowest numeric value has the highest priority. The event encoder module converts event trigger inputs into RHIC event codes in a translation table. The translation table can be read and written via the VME interface.

INPUT MODULES

Each event input module accepts up to 16 event trigger inputs, and determines their relative priority. If other event input modules have been triggered, the event input module must have position priority (closest to the encoder module) in order to place its event trigger code on the bus. Sixteen input modules are required to support 256 events.

Event triggers can originate from software initiated commands to an input modules CSR or hardware generated pulses.

There is a 1.3 μ s event code transmission delay built into system. This assures that very high priority events will be transmitted with minimum time jitter. It is possible for a low priority trigger to be delayed by higher priority triggers. In this case there may be several transmission increments (1.2 usec/increment) from the trigger until the event is transmitted on the RHIC event link.

V102 DECODER/DELAY MODULE

The RHIC V102 module is a general purpose decoder/delay module that can be used to provide timing to systems and equipment not having a direct connection to the RHIC event link. The form factor is a 4hp X 6U VME module. The V102 includes a direct connection to the event link and has a VME interface for setting

up and configuring each delay channel. Each module contains eight output channels with flexible triggering and delay options. Delay clocks can be either internal or external.

V102 Module Functions

The V102 derives a 10 MHz clock from the RHIC event link carrier. Internal clocks are divided down from the 10 MHz clock. The divider chain may be synchronized to a user specified event code.

Each of the delay channels can be triggered from event link event(s) or, the preceding event channel (an external trigger coupled by an external cable in the case of channel 1), or an external trigger input.

A separate delay is provided for each channel. The delay is developed in a 32-bit counter, programmed to count down. The minimum delay is 1 count. The channel delay clock may be selected from the 10 MHz or 1 MHz internal clock or the external clock input. If an external clock is used, the maximum frequency is 5 MHz.

The output pulse width is controlled by a 16 bit counter, programmed to count down. The minimum pulse width is one delay clock period. The clock rate selected for the delay function is used for the pulse width counter.

Event channel outputs are available on the front panel and rear VMEbus P2 user pins. All triggers, event link event, VMEbus, or external are synchronized to the selected clock (external or internal) before the delay count down begins. Each decoder/delay module is completely self supporting, once initialized.

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