UPGRADE OF NSLS TIMING SYSTEM *

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I. ABSTRACT

We report on the progress of the new NSLS timing system. There are three types of requirements for NSLS timing system: clocks, synchronization and trigger circuits. All ring revolution frequency clocks are generated using ECL and high speed TTL logic. The synchronization circuits allows to fill both storage rings with any bunch pattern. The triggers are generated by using commercially available digital delay generators. The delay unit's outputs are ultrastable, with a resolution of 5 ps, and are programmed by computer via IEEE 488 interface. The block diagrams, description of all major timing components and the present status are provided in this paper.

II. INTRODUCTION

Electrons are injected into the NSLS storage rings from a 750 Mev booster synchrotron fed by a 120 Mev linac [1]. Each injection cycle populates one bunch into the booster, which then is extracted into either storage ring. The multibunch fill is achieved by sequencing the injection/extraction cycle to all bunches, one bunch at a time.

The NSLS timing system was commissioned in 1979 [2], which did not include the control for the single bunch transfer. In 1982, this function was added as an add-on timing system (single bunch transfer system [3]) which is controlled by its own microprocessor [4]. Although, this hybrid timing system has provided single bunch transfer operation, routinely, but it has become complex and difficult to maintain. The reliability has been poor and, occasionally, the timing jitter has been high.

The new timing system is simple and integrated; and is described in the following sections. Following data are useful in understanding the timing system:

UV rf frequency = 52.8856 Mhz
X-ray rf frequency = 52.8875 Mhz
Booster harmonic number = 5
UV harmonic number = 9
X-ray harmonic number = 30.

III. CLOCKS

The figure 1 provides the block diagram for clock generating circuits. The storage ring harmonic counters are free running and generate UV revolution clock (uvrf/9) and X-ray revolution clock (xrrf/30). The booster ring harmonic
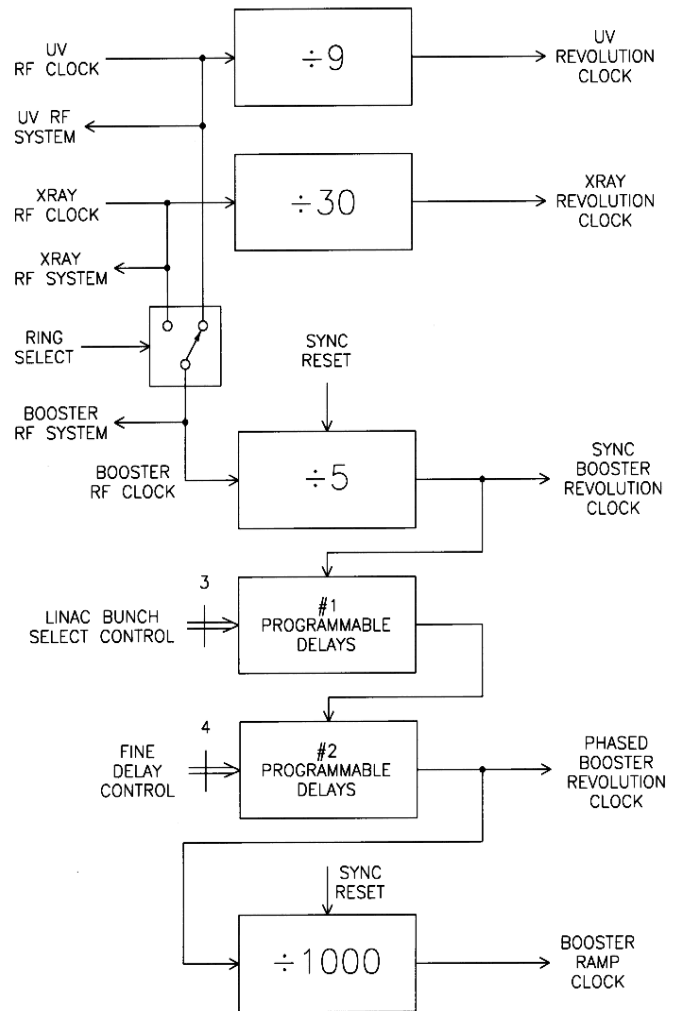

Figure 1 - Block Diagram for Clocks Circuits

counter generates booster revolution clock (brf/5) which is synchronized to the storage ring bunch marker (brf/90) by a sync reset signal. This synchronization, discussed more later, is necessary because when a new ring is selected to fill (changing the rf clock to the counter), the sync is lost.

Next, this clock (sync brf/5) is sent to the programmable delay (# 1) which provides 5 equally spaced delays. Each delay step is equal to the rf time period and it allows to select all five phases of brf/5 clock, precisely. Further, this clock is fine tuned by another programmble delay (#2). The setting resolution of this delay is ~ 1 nsec, which allows to tune the phased brf/5 clock to the linac.

The last counter (/1000) generates ~ 10 khz clock, which is used by booster ramping power supplies.

IV. SYNCHRONIZATION

The synchronization circuits consist of one delay unit DG535, few flip-flops and gates, as shown in figure 2. The delay section A generates injection repetition clock (Trep), with time period selectable in increment of 1/60 sec. A 60 hz line signal triggers this delay section, while the delay is programmed to few msec less than desired repetition rate. Two additional clocks, Tphase1 and Tphase2, are generated from Trep. Tphase1 clock, delayed by ~ 20 msec from Trep, is synchronized with the storage ring bunch marker (brf/90), generating sync reset. Tphase2 clock, delayed by ~ 1msec from

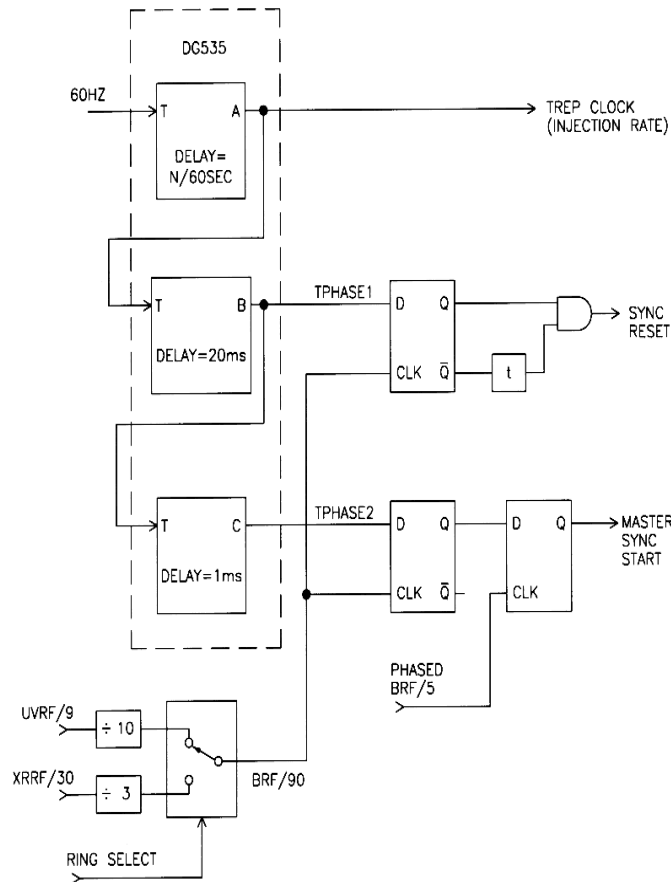Tphase1, is synchronized with the storage ring bunch marker (brf/90), as well as, with the linac bunch clock (phased brf/5). This generates a master sync signal, which is used to trigger all other triggers as described in the "TRIGGER' section. This ensures that all trigger output are in phase with the linac bunch.

The storage ring bunch marker clock (brf/90), is generated as shown in the synchronization circuits.

Figure 3 shows the relative timings of above described signals and the sequence of events occur as follows: the Trep clock generates a flag for the computer, signaling, that it has next 20 msec for loading any new delay values into the injection delay units. Also, during this time, the booster bunch is selected, when computer selects one of five programmed delays in delay # 1 shown in the figure 2. Sync reset signal, generated by Tphase1 is used to reset the booster counter. The master sync signal, sequenced by Tphase2 signal, is used to trigger all delay units described in the TRIGGER section.
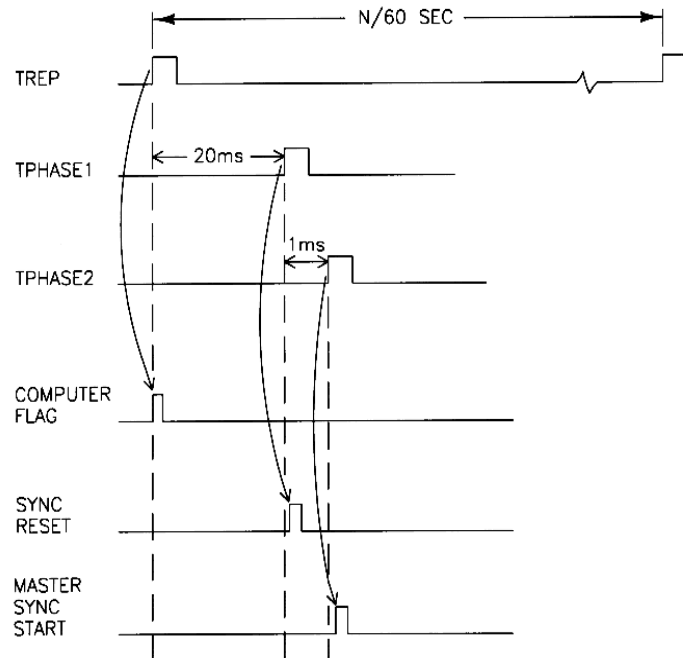

Figure 3 - Timing diagrams

V. TRIGGERS

All triggers are generated by ultrastable, low jitter programmable delay units. These delay units (DG 535 - Stanford Research Systems) are available, commercially, and the output delays can be set via IEEE 488 interface. Each delay unit is programmed to trigger from an external signal and provides upto four independent programmable outputs (A,B,C and D). The output jitter is lower than 0.5 ns and each

Figure 2 - Synchronization circuits

delay can be set with a resolution of 5 psec, if needed.

Figure 4 shows the layout of 6 delay units, which are grouped based on functions. The master sync signal, generated by sync circuits, triggers the top delay unit generating three START triggers: start of linac (TSOL), start of booster (TSOB) and start of ejection (TSOE). TSOL output triggers a group of two delay units providing signals used for linac gun, klystrons and linac to booster injection bumps/kickers. TSOB output triggers one delay unit providing signals for starting ramps for booster power supplies. TSOE output triggers another group of two delay units generating all trigger timings for ejection bumps and kickers.
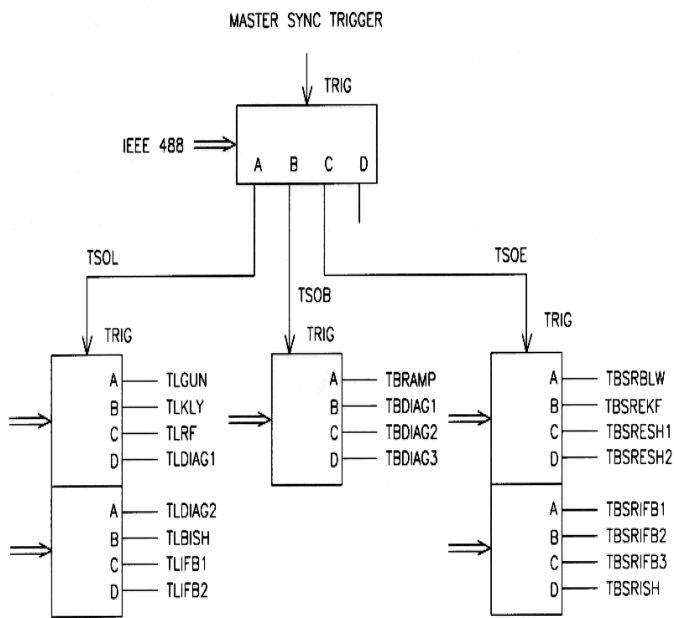

Figure 4 - Triggers block diagram

VI. STATUS

The computer interface to four delay units has been tested with an update request rate of 2 hz. The test has been successful and have demonstrated that all delays, required for injection/ejection, can be updated in less than 20 ms. The synchronization logic and clock circuits have been built and are being tested. The fast trigger distribution amplifiers are under construction, which will be used for driving triggers at their locations. The preliminary test on the complete system will start within a month and it is expected that the new system will be operational soon after that
.

VII. ACKNOWLEDGEMENTS

VIII. REFERENCES

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[4] S. Ramamoorthy, J.D. Smith, O. Singh - Multibunch controls ,NSLS Technical note # 170 - 1985