Fermilab Main Ring Low Level RF System Modifications For Focus Free Transition Beam Tests

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Abstract

A novel idea for crossing transition energy has been proposed for study in the Fermilab Main Ring accelerator. The idea has been named focus free transition crossing[1] and involves reducing the RF focusing force nearly to zero when the beam energy is near the transition energy by adding a third harmonic to the RF accelerating voltage, and then adjusting the accelerating phase angle to 90°. The modification of the accelerating voltage wave form shape and phase are accomplished by accurate program control of the amplitude and phase of the 53 Mhz RF cavities and a recently installed 159 Mhz cavity. The studies also require interrupting the normal LLRF system beam energy feedback loops in favor of a new energy control loop near the transition energy. This paper describes the functions of the LLRF system electronics recently installed to facilitate this control, and initial operational experience with the system.

Introduction

Focus free transition crossing (FFTC) may offer an improvement in Main Ring performance through reducing longitudinal emittance growth and beam loss as beam accelerates through the transition energy. The basic concepts of focus free transition crossing and performance improvements, plus some results of recent beam studies are described elsewhere.[2,3] The Main Ring LLRF system modifications[4] discussed here are to control the 53Mhz RF cavities and a recently installed 159Mhz RF cavity very accurately in amplitude and phase. This produces an accelerating voltage wave form with zero slope around 90°, and thus provides only the required accelerating voltage with no RF focusing force. This control occurs during the non-adiabatic period around transition, an interval of approximately 10 msec. The new LLRF system operating modes for focus free transition studies in no way compromise existing operation.

Background

Even without functionality required for FFTC studies, the Fermilab Main Ring LLRF system is a complex beam control system providing an interesting variety of control options for the Fermilab physics program. The LLRF system accommodates RF synchronous transfer of beam from several machines, accelerates protons or antiprotons, operates on different MR ramp profiles and peak energies, and provides bi-directional beam transfers to specific RF buckets between MR and Tev at 150 Gev. The MR LLRF system uses a VCO and signals from two beam detectors to control the beam energy. Beam signal from a stripline longitudinal detector located at F11 is processed and serves as the master input to phase lock loop feedback which forces the VCO to follow the beam frequency and damp coherent energy oscillations at the synchrotron frequency. Signal from a horizontal position detector at F28 is processed to provide a beam radial position measurement (RPOS) that is compared to a desired position program (M3ROF). The resulting position error signal (RPERR) is processed and drives a phase shifter to control the beam accelerating phase angle and energy gain per revolution. When FFTC studies produce an accelerating voltage with zero slope, the radial position feedback loop can no longer use the accelerating phase angle to control the beam energy, and is abandoned in favor of a loop using the RF amplitude to control energy.

The MR LLRF also controls the RF bucket area for bunch shape manipulations at flattop energies.[5,6] These manipulations accomplish bunch rotation at 120 Gev for pbar production, and bunch coalescing at 150 Gev for Tev injection in the Fermilab colliding beams physics program. For bunch rotation and coalescing, the MR LLRF output and the RF cavities are divided into A and B groups, and the system independently controls A and B group amplitudes and phases. Application program T101 calculates voltage and phase programs and loads these into four sets of Camac 069/071 digital curve generators. The phase programs are a single 12 bit curve that input to the Counterphase Program Select module (CPPS), which receives timing information to select when programs play. The CPPS module 12 bit outputs drive two phase shifters called Counterphase A and B modules. The Counterphase modules are a specific application of hardware widely used at Fermilab called DF modules. They are digitally controlled, bi-directional, fully periodic RF phase shifters providing phase resolution of .09°. The existing T101 phase programs, the CPPS module, and Counterphase shifters equally retard and advance the A and B group phases respectively. This system also provides the operational transition phase jump. A CPPS digital input named M:TPJEnn ("nn" is a MR cycle type) specifies a phase jump magnitude, and equally advances the A and B group phases at transition. FFTC studies require individual A and B phase programs to simultaneously counterphase A and B LLRF outputs while also advancing the A+B sum voltage phasor to 90°. Existing phase programming could not satisfy this requirement.

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Digital Adder module

The Digital Adder was designed to provide new A and B group phase programming for FFTC studies, and is in series between the existing CPPS and Counterphase modules. The adder has two channels of processing with two stages of ALUs in each channel. It combines three new digital phase control inputs with the two CPPS A/B phase programs. These 5 inputs produce 2 digital outputs which drive the Counterphase A/B shifters. Two of the new inputs are named M:PPGA and M:PPGB (Phase Program Group A and B). These provide unique A and B group program curves for FFTC studies and are generated in Camac 467 modules. Application program W48 derives required PPGA and PPGB phase programs and loads the curve generators[7]. The third new phase control input is named CPEFB, for CounterPhase Energy FeedBack. This input provides small counterphase angle modulation between the A and B groups to control the beam energy during the FFTC interval and will be discussed later.

The two Digital Adder phase control outputs and the resulting phase shifts generated by the counterphase A and B shifters are:

$$\Phi_A = -CPPSA + PPGA - CPEFB$$
$$\Phi_B = +CPPSB + PPGB + CPEFB$$

The sign convention is that positive $\Delta\Phi$ is phase advance.

The Digital Adder has the following features. All inputs and outputs are 12 bits and have an associated data valid strobe. All input and output data is latched in the Adder. The Adder asynchronously combines all active input data in a method which guarantees maximum throughput and correct output. The maximum throughput is when only one input is active and corresponds to a delay of 260 nsec. The slowest data output rate occurs when all three inputs are active with no timing overlap, corresponds to the largest delay between a first input data change and output update, and results in a delay of 780 nsec. The Adder does not have on/off gating, and includes no provision to reset output data. The system relies on Adder input data sources to properly reset Counterphase A/B shifter program inputs to appropriate values (generally 0°) when programs finish.

Digitize/Hold modules

The MR LLRF system has two Digitize/Hold modules which provide two (of four possible) channels of functionality required for FFTC studies. A Digitize/Hold module features two channels with input buffering and scaling options, track and hold, 12 bit 600 Khz ADC, digital output (Dout), and reconstructed analog output (Vout). The module provides true 12 bit resolution and all bits are used. Channel 1 accepts ±10 volt signals and is scaled so Vout = Vin. Channel 2 accepts +/- 2.5 volt signals and is also scaled so Vout = Vin. Channel encode rate can be separate or common, and the clock source can be internal or external. In the FFTC application, the digitize rate is common for both channels and is from an internal 500 Khz TTL clock oscillator. Each Digitize/Hold channel accepts a TTL active high Hold control input gate. Module timing is designed so that Dout and Vout remain constant at their last value before the positive edge of the hold gate. The modules are used as accurate track and infinite hold circuits. Since the ADC always runs, Dout and Vout quickly reacquire Vin at the hold gate negative transition.

Counterphase Energy Feedback

The two Digitize/Hold channel Vin signals used for FFTC studies are both from the LLRF system radial position (energy) feedback loop. The ± 10 volt channels of two Digitize/Hold modules are used. One channel digitizes the loop output signal (M:PSHIFT) to the loop phase shifter. This digitizer is simply in series with the PSHIFT signal, and delivers Vout to the loop phase shifter. The second channel digitizes the RPERR signal from a point early in the Radial Position Feedback Loop Processor module. Dout from this Digitize/Hold channel is in 2's complement format and represents the beam energy error. At the beginning of the FFTC interval, a hold command is given to the PSHIFT digitizer. This holds M:PSHIFT and the RPOS loop contribution to the beam acceleration phase angle constant, establishes the initial conditions for subsequent phase programming, and effectively opens the energy feedback loop normally used during acceleration. PPGA and PPGB phase programs then counterphase the A and B RF cavity groups while advancing the acceleration phase angle to 90°. The typical initial counterphase angle is 55°, and is called the cone angle. Dout from RPERR is the CPEFB phase control summed by the Digital Adder into the Counterphase A/B shifter inputs. CPEFB modulates the cone angle between the A and B RF cavities and the amplitude of the flattened RF voltage wave form. This provides beam energy feedback during the FFTC interval.

The total cone angle modulation by the CPEFB loop input must never exceed the programmed cone angle between the A and B RF cavity groups. This would reverse the sign of the feedback loop and destroy the beam if allowed to adjust the beam energy gain per turn too much, and means the CPEFB loop contribution to A and B phase programs must be limited to one half the programmed cone angle.

Digital Limiter module

This module receives the digitized RPERR output data (Dout) from the CPEFB loop Digitize/Hold module. The Digital Limiter sets upper and lower limits on the CPEFB loop cone angle modulation to avoid positive feedback. The limits are currently set to ±22.5°.

The circuit consists of PLS153 program logic array's which determine if the 12 bit input phase program is within allowed limits. Dual 4 - 1 data selectors/multiplexers (74LS153's) either pass the input or an upper or lower limit value. The final output stage uses 74LS541's output drivers. The module also outputs a data valid strobe to latch information into the Digital Adder. Module output data is active only when a TTL control gate input is high. The gate

is generated from system triggers named M:TCPFON and M:TCPFOF (CPEFB ON and OFF). At M:TCPFOF the Limiter module outputs 0° and a data valid to reset the CPEFB Digital Adder input.

RF Rephaser Module

This module receives the 53Mhz LLRF A and B group outputs from the Counterphase A/B phase shifter modules. Both inputs are amplitude limited and processed to produce an RF output that is constant amplitude, and at the phase of the vector sum of the A and B RF inputs. The advantage of the Rephaser output is that it represents the phase of the 53Mhz RF sum voltage by a large amplitude signal, even when the A/B shifters are programmed to counterphase the true sum vector amplitude to a very small value. The RF Rephaser output drives the 159 Mhz oscillator.

159 MHz Oscillator

This module receives the RF Rephaser module signal, amplitude limits the input with a 20 dB range AGC circuit, and triples the frequency. The module 159Mhz output drives the 159 Mhz amplifier system and RF cavity[8]. An input curve named M:HV3PG from a Camac 465 module programs the RF output amplitude and the cavity voltage. The RF output is turned on and off by a TTL gate controlled by system triggers named M:TH3ON and M:TH3OFF.

The 53 Mhz input from the Rephaser module is already constant amplitude, but to facilitate using the 159Mhz oscillator in other applications it has an input AGC circuit. The AGC circuit is an AD834 multiplier transformer coupled to a Comlinear current feedback operational amplifier. The amp output is AC coupled and drives a power splitter and simple diode detector. The detector output is viewed at a monitor called Vdet. Vdet is compared to Vset, an internal set voltage, and produces an error signal for a high gain feedback loop that controls the multiplier gain input.

The AGC circuit 53Mhz output drives a simple frequency tripler consisting of two power splitters, an RF amplifier, and two mixers. Mixing products are removed by a Trilithic 4BC159/10-3-CC tubular band pass filter.

The oscillator is capable of two types of feedback operating on the 159Mhz cavity voltage. The feedback is enabled by system timers M:TH3FON and M:TH3FOF. The first type is 159/53 Mhz amplitude ratio feedback. It forces the detected 159Mhz cavity voltage to equal a specified fraction of the detected 53Mhz cavity voltage. The second feedback type is direct feedback and forces the detected 159 Mhz cavity voltage to follow the amplitude input program HV3PG. This loop would compensate for gain changes in all components of the 159Mhz amplifier system. During FFTC studies the 53Mhz RF cavity voltage is modulated by the CPEFB loop and PPGA/B programming. The 159Mhz cavity must maintain the correct voltage ratio (approximately 13% of the 53Mhz) to optimize the RF wave form flatness. Selection of feedback loop type is via a jumper option. Ratio feedback is currently implemented.

Oscillator performance summary

Max. RF input:	+7 dbm
AGC stage RF input range:	-15 to +5 dbm
Input frequency:	500 Khz to 80 Mhz
Vset	- 1.563 volts
AGC stage RF output:	+ 3.4 dbm

Conclusion

All the hardware necessary for focus free transition crossing beam studies is implemented in the MR LLRF system. Curve genenerators and application program W48 are used to control the hardware with predicted accuracy and results. FFTC beam studies verify correct control of the MR 53Mhz and 159Mhz RF cavity amplitudes and phases. Control of the beam energy in the FFTC interval with the new feedback loop works well. A key signature of successful FFTC is bunch length increase (instead of shortening), and no beam loss through transition. This signature has been observed routinely during FFTC studies.

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