Study of Porous Silicon Morphologies For Electron Transport*

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Abstract

Field emitter devices are being developed for the gigatron[1], a high-efficiency, high frequency and high power microwave source. One approach being investigated is porous silicon, where a dense matrix of nanoscopic pores are galvanically etched into a silicon surface. In the present paper pore morphologies were used to characterize these materials. Using of Scanning Electron Microscope (SEM) and Transmision Electron Microscope (TEM) images of both N-type and P-type porous layers, it is found that pores propagate along the $< 100 >$ crystallographic direction, perpendicular to the surface of (100) silicon. Distinct morphologies were observed systematically near the surface, in the main bulk and near the bottom of N-type (100) silicon lift-off samples. It is seen that the pores are not cylindrical but exhibit more or less approximately square cross sections. X-ray diffraction spectra and electron diffraction patterns verified that bulk porous silicon is still a single crystal. In addition, a Scanning Tunnelling Microscope (STM) and an Atomic Force Microscope (AFM) were successfully applied to image the 40 Å gold film structure which was coated upon a cooled porous silicon layer. By associating the morphology study with the measured emitting current density of the Oxidized Porous Silicon Field Emission Triode (OPSFET), techniques for the surface treatment of porous silicon will be optimized.

I. INTRODUCTION

Yue[2] demonstrated that diodes formed using porous silicon films can sustain remarkable transconductance, that the process is field emission, and that the emitted electrons are transported in the vacuum pores of the material. He dubbed this device the Oxidized Porous Silicon Field Emission Diode (OPSFED). Both N- and P-type silicon with different orientations and doping concentrations were used to investigate field emission properties of the OPSFED. Further study [3] showed that the OPSFED field emission current density was higher with P-type than with N-type silicon. With an operation voltage of less than 20 V, the current density reached more than 100 A/cm^2. Next, an Oxidized Porous Silicon Field Emission Triode (OPSFET) was developed with P-type (100) silicon, anodized with current densities from 40 mA/cm^2 to 70 mA/cm^2. In order to obtain a smooth gold layer over the porous silicon but keep the fine pores open, a thin gold film was evaporated onto the porous silicon substrate that had been cooled to liquid-nitrogen temperature. The gold film serves as a gate electrode in the OPSFET to obtain high electronic field strengths for extracting electron emission efficiently. The morphology study presented in this paper is aimed at providing a technological means to distinguish differences in morphologies of the porous silicon samples that were prepared under the same conditions as the porous silicon for OPSFED's and OPSFET's were fabricated.

II. SAMPLE PREPARATION

The porous silicon samples for morphology study were all anodized in an anodization cell with a 1:3 mixture of 99% wt. ethanol : 49% wt. HF solution. After baking at 65°C for 10 minutes all the samples were pumped down to 10^{-7} Torr vacuum overnight for evacuating the residual HF solution from the pores. Afterwards, samples prepared for SEM, AFM and STM were oxidized in the furnace at 845°C for 45 minutes. STM samples were placed onto a substrate cooled to 77°K and coated with 40 Å gold by thermal evaporation. Both P-type and N-type (100) silicon were investigated.

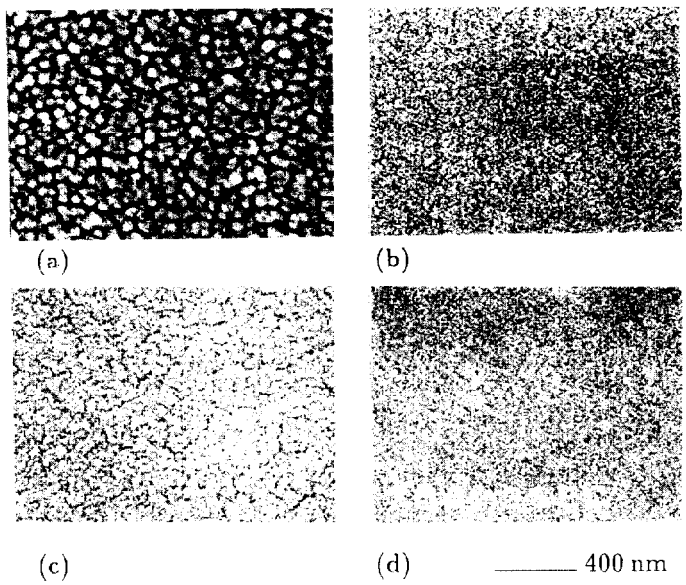

Fig.1 Plan-view SEM images of porous silicon samples before and after RIE. (a) and (b) P-type (100), 0.01 Ω cm, anodization current density is 40 mA/cm^2, (a) after 2 min RIE, (b) before RIE. (c) and (d) N^+-type (100), 0.001 Ω cm, 75 mA/cm^2, (c) after 1 min RIE, (d) before RIE.

The instruments that we have used in our experiments are: SEM: JEOL 6400; TEM: Zeiss 10C, JEOL

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2010; AFM: Nanoscope 3; STM: Nanoscope 2; RIE: Drytech DRIE-100; and Dual Ion Mill: 600 series.

III. EXPERIMENTS AND RESULTS

A. Porous silicon in the top layer and main bulk

Fig.1(a) and Fig.1(c) show the plan-view SEM images of the N^+-type porous silicon surfaces after reactive ion etching (RIE) for 1 minute and 2 minutes respectively by using SF_6 gas at a flow rate of 7 sccm, a power of 200 W and a bias of -550 V. RIE etches the top porous layer about 600 Å /min. The etched thickness was measured using an ALFA stepper. Comparing SEM images before and after RIE etching, it is seen that N^+-type oxidized porous silicon has different pore densities between the top surface layer and the main bulk.

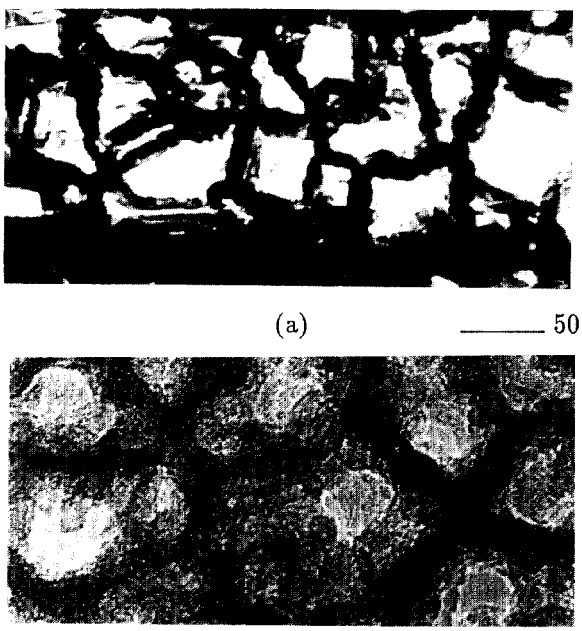

Fig.2 Plan-view TEM images. (a) N^+-type porous silicon lift-off sample, 0.001 Ω cm, near lift-off side. (b) P^+-type porous silicon, 0.001 Ω cm, anodization current density: 60mA/cm^2

B. Pore shape and propagation

The lift-off technology was used in preparing samples. Anodization was ended by slowly increasing anodization current to 350 mA/cm^2 for 1 minute so that the porous silicon membrane was lifted off from the substrate. Fig.2 (a) shows a TEM plan-view image near the lift-off side made from N^+-type silicon. Pores in this view exhibit mostly square cross-section. Fig.2 (b) shows a TEM plan-view image made from P^+-type silicon. It is found that pores propagate along the $<100>$ crystallographic direction, perpendicular to the surface of (100) silicon wafers. A similar result was reported by Chuang and Smith [4]. The porous silicon formation mechanisms were discussed by Smith and Collins [5].

C. Pore size and density

Samples from P^+-type, 0.001 Ω cm, (100) silicon wafers ("P^+") were anodized at current densities of 20mA/cm^2, 40mA/cm^2, 60mA/cm^2 80mA/cm^2 and 150mA/cm^2 respectively. These samples were investigated by TEM and AFM. Fig.3 shows pore sizes in cross sectional TEM (XTEM), increasing with the anodization current density. The pore sizes and densities were measured from both cross sectional and plan-view TEM images, and are listed in Table 1. TEM electron diffraction pattern and X-Ray diffraction spectra indicate that porous silicon is still single crystalline.

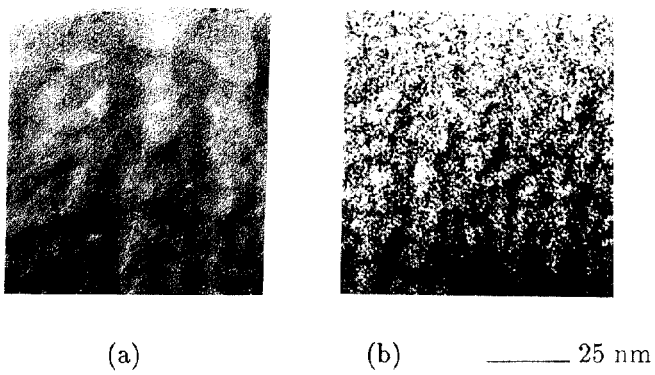

Fig.3 XTEM images of P^+ porous silicon. (a) anodization current density 150mA/cm^2. (b) anodization current density 80mA/cm^2.

Table 1 Pores size and density in porous silicon

doping type	anodization cuurent density (mA/cm^2)	pore size (nm)	pore density (10^{11}/cm^2)
P^+	150	5 - 16	2 - 5.0
	80	4 - 11	2 - 4.5
	60	4 - 9	2 - 4.5
	40	3 - 8	2- 3.5
	20	3 - 6	
N^+	60	4 - 6	6 - 7

D. Structure of gold gate electrode layer

A 40 Å gold film was coated onto the surface of porous silicon by thermal evaporation in a 10^{-8} Torr oil-free vacuum chamber [6]. The substrates were cooled to liquid-nitrogen temperature during the coating process. The low temperature is expected to limit migration of deposited gold atoms, preventing formation of islands and thereby creating a smooth thin film. This technology has been successfully used with various kinds of dielectric substrates [6]. The coated gold thin film is used as a gate electrode layer, which could be used to extract emitted elec-

tron current from the porous silicon to the anode if those pores remain open after coating. Porous silicon devices which were used in OPSFET's were chosen from those wafers that demonstrated high emission current densities at low operation voltage in OPSFED's.

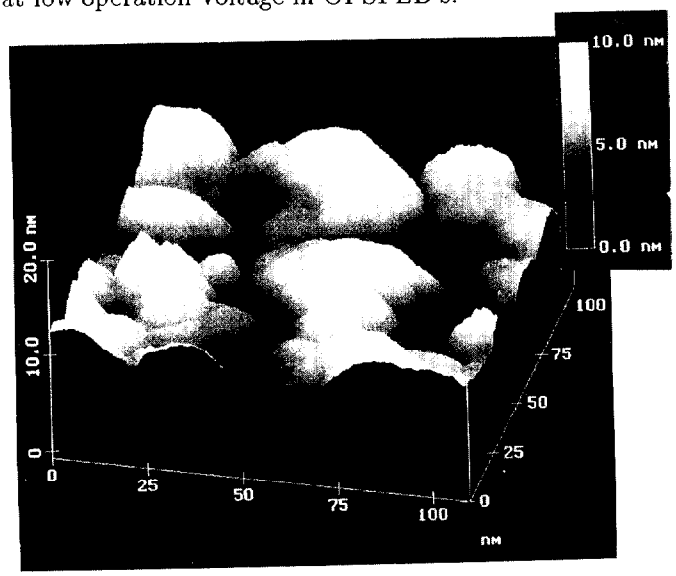

Fig.4 STM image of 40Å Au layer on P^+ porous silicon, 40mA/cm^2

Fig.4 shows a STM image of the thin gold film coated on the porous silicon which was anodized with a current density of 40 mA/cm^2 in 30% HF solution. Apparently, this coated surface is smoother than the normal coating but still small (~25 nm) gold islands were formed. The TEM plan-view image for the same kind of sample shows that the average size of pores is about 5 nm (Fig.5). By comparing the STM image with the TEM image it can be seen that the gold islands cover some pores and the thin film is not completely continuous. It is speculated that non-uniform deposition may have been caused by an increase in the surface chemical potential during the electrochemical anodization process. Further study is necessary to improve gold deposition on porous silicon and thereby to enhance the efficiency of field emission into vacuum.

IV. CONCLUSION

P^+ (100) porous silicon shows high field emission properties when produced with an anodization current from 40 mA/cm^2 to 70 mA/cm^2. The densities of pores are 2-5$\times$10^{11}/cm^2, pore sizes are 3-10 nm, the pore walls are 5-12 nm in those porous silicon samples. Pore structures exposed with XTEM appear as small channels with numerous "budding" side branches. Those fractal branches form tiny sharp tips with nanometer sizes, which may be the origin of field emission current. Efforts are being made to deposit a gold gate layer upon the porous silicon without plugging pores. Cold gold evaporation and surface treatment to reduce the surface chemical potential are being studied.

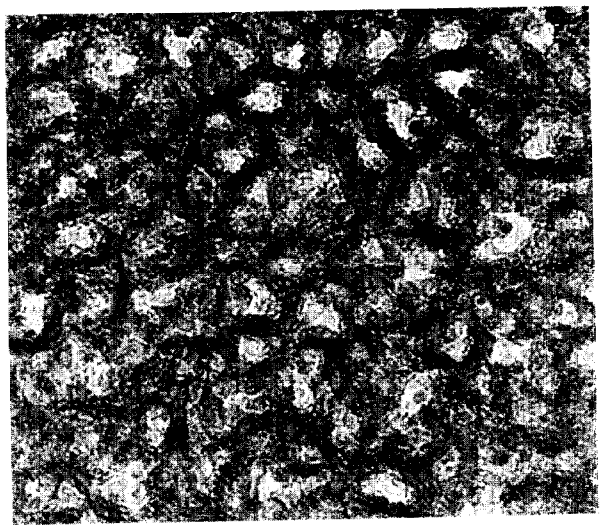

Fig.5 Plan-view TEM image of P^+ porous silicon, 40mA/cm^2

V. ACKNOWLEDGEMENTS

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