A Digital Phase and Amplitude Feedforward Correction System*

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Abstract

We have designed and fabricated a phase and amplitude correction system[1] (PACS) using digital microelectronic circuitries and microstrip RF components with subnanosecond switching and response time. The control system uses a feedforward scheme to correct unwanted variations in phase and amplitude of a short (<100 ns) RF pulse which is generated repeatedly by an external RF source (e.g. relativistic klystron, FEL). Programmable or constant phase and amplitude (to within 0.5° and 0.1 dB, respectively) are achievable with the PACS. The system features a digitally programmable phase shifter and attenuator based on a direct RF digital-to-analog converter[1] (RFDAC).

Introduction

RF phase and amplitude stability is critically important for many accelerator applications. Devices for producing repeatable pulses of microwave energy at very high peak power typically include a pulsed microwave amplifier which amplifies an input signal produced by a low-power microwave generator. The energy required for signal amplification may be derived from a high energy electron beam directed into the amplifier. Klystrons, relativistic klystrons, free electron lasers and cyclotron auto-resonant masers are examples of pulsed microwave amplifiers of this kind. Amplitude and phase stability at the output of such pulsed microwave amplifiers is strongly dependent on the stability of the current and voltage, respectively, of the driving electron beam. For certain electron drivers such as linear induction accelerators, it is difficult to eliminate the current and voltage variations in a given pulse. Because of the physical sizes and resulting long signal paths of these devices, feedback correction techniques are not fast enough to correct variations in the phase and amplitude of the output *during* each pulse. An analog feedforward correction system[2] was considered earlier but was abandoned because, among other reasons, voltage-controlled phase shifters and analog output switches were too slow.

Our approach here is to use a fast digital feedforward correction system to incrementally reduce phase and amplitude variations in successive pulses. The apparatus comprises 1) a module which detects the phase and amplitude of an RF output pulse as a function of time, compares them with those of a reference, and converts the analog error signal into a sequence of 1-bit error data, 2) a module which stores and processes the phase and amplitude error data to generate two separate sequences of N-bit correction words, and 3) a module which uses the correction words to modulate the phase and amplitude of subsequent pulses. Since the pulse width (<100 ns) is typically much shorter than the time between pulses (>10 ms at moderate rep rate), the error detection and correction (modules 1 and 3) require very fast, accurate and reliable circuitry, while the error processing (module 2) can be done at a much slower clock rate between pulses. The system functions are synchronized by timing and control logic. The portable system is designed to mount in a standard 19 inch drawer, complete with power supply and self test logic. We plan to test this system soon on a high-power choppertron at Lawrence Livermore National Laboratory.

Description of the System

Fig. 1 is a functional block diagram of the phase and amplitude correction system (PACS). The system modifies the RF input signal based on error information obtained from the high power amplifier output. A portion of the RF CW input signal is used to provide a phase reference for the PACS. Another portion, after being modified by the PACS, is used to drive a high power amplifier such as a choppertron. The output frequency (11.4 GHz) of the LLNL choppertron is twice that of the input (5.7 GHz).

A small amount of the RF output pulse power is transported via a directional coupler to the PACS for processing. This signal is divided by a splitter and applied to a phase detector and an amplitude detector. The frequency of the phase detector reference is doubled to be coherent with the RF feedback pulse. An adjustable line stretcher is used to calibrate the phase detector.

An internal clock driven by a 1.5-GHz oscillator controls the timing bin width and the number of bins during a pulse. For the prototype PACS, we divide a pulse into 18 bins each having a bin width of 4 ns. The starting time of the first bin is within 1/3 the bin width, or 1.33 ns.

Analog phase and amplitude error signals are converted to logic levels, bin-to-bin, by two separate comparators. Reference voltages or thresholds for the comparators are individually adjustable with potentiometers. The comparators may be considered to be 1-bit analog-to-digital (A/D) converters. A third comparator produces an input timing synchronization pulse. The amplitude error threshold is independent of the input timing threshold. A fourth comparator produces the output timing synchronization pulse. The input to the fourth comparator is provided by an external timing pulse. This pulse is timed so that its leading edge causes the phase and amplitude correction signals to arrive at the input of the high-power amplifier at the appropriate time to correct the output pulse.

The system corrects the phase and amplitude errors in parallel. Each pulse is divided into M bins. There are as many error (1-bit) words and correction (N-bit) words as there are bins. For the prototype, M=18 and N=6. Each of the 1-bit error data indicates whether the detected phase or amplitude in a time bin is higher or lower than the reference in the same time bin. The phase and amplitude errors are stored for each cycle and processed between pulses to generate the correction data for the next cycle. The algorithm for the mechanization is to either add one to a correction word, or subtract one from it, according to the sign of the corresponding error word. Shift registers are used for error and correction data storage. A timing signal consisting of M bursts of pulses are applied to write or read the M words of a pulse.

During the processing cycle, the error data in the storage banks is read out by applying slow clock bursts (approximately 1 MHz) of M pulses and processed by the correction logic. The results are stored in storage banks via a multiplexer. During the correction cycle, the correction data is shifted out of storage banks by applying the fast clock bursts, and applied separately to a programmable phase shifter or a programmable attenuator. The RF input is first corrected by the phase shifter, and is then coupled to the attenuator where the amplitude is corrected. The attenuation of the phase and amplitude correctors in the prototype system is chosen to provide a phase correction range of ±30° in approximately 0.5° steps, and an amplitude correction range of ±3 dB in approximately 0.1 dB steps. Finally, the PACS output is applied to an external circuit as an RF input to a high power amplifier.

Timing and Control

The fundamental timing of the PACS is shown in fig. 2. The cycle is started by an output timing pulse. The correction cycle or fast output clock bursts are initiated by the leading edge of output timing pulse, and the processing cycle or slow clock bursts by the trailing edge. The output timing pulse is approximately 2 microseconds in duration to allow for completion of the correction cycle before starting the data processing cycle. The RF feedback pulse appears at the corrector system some time after the output fast clock bursts. The input timing pulse occurs when the RF output pulse is detected by the amplitude detector and comparator, triggering the input fast clock bursts. The fast output clock bursts can be delayed to compensate for differences in the phase and amplitude error detection paths.

The M slow clock bursts of the data processing cycle are initiated after the completion of the correction cycle. In the prototype PACS, the slow error processing logic block is time-shared by the phase and amplitude correctors.

The input timing logic and output timing logic are identical in generating the fast clock bursts of M pulses, but operate independently in time. They are driven by the high frequency clock generated by the 1.5-GHz oscillator. The frequency of this clock is 6 times the bin rate. The bin-rate clocks are derived by dividing-down the frequency of this clock. Since the clock bursts are started on any cycle of the clock, the granularity of synchronizing the bin clocks with the actual bins is a fraction of a bin-time.

Programmable Phase Shifter and Attenuator

A feature of the present system is the provision of very fast bin-to-bin switching in the phase shifter and the attenuator. For this purpose we have conceived and implemented an RF digital-to-analog converter (RFDAC). The basic idea of the RFDAC[1] employs mixers that are digitally controlled as bi-phase modulators producing binary weighted outputs, which are then summed to produce the desired output amplitude. Schottky diodes possess the properties of high-speed switching and meet the drive requirements. The output voltage is an RF signal rather than the conventional DC. The RFDAC is thus an apparatus which produces the processed RF directly without intermediate analog steps. A schematic of a 6-bit RFDAC is shown in fig. 3. Leads 2 and 4 are RF input and output, respectively. Lead 3 is a digital input. Prior to assembling the phase and amplitude correctors, we dynamically staircase tested a 6-bit 5.7-GHz RFDAC breadboard, monitoring the RF waveform with a Tektronix 11802 sampling scope. A control logic circuit triggers a total of 64 steps in 180 ns (2.8 ns/step). A band-pass filter of 2.4 GHz bandwidth centering at 5.7 GHz is used to suppress logic noise feedthrough. The dynamic test setup is shown in Fig. 4 and the staircase test results are shown in fig. 5.

A simple way to implement a programmable attenuator using an RFDAC is shown in fig. 6. The RF input is split by a power splitter and applied to the input of an RFDAC and to a power combiner. The output of the RFDAC is applied to the same combiner. The RFDAC produces an RF output according to the state of the digital input. The output voltage of the combiner is equal to 0.7071 times the vector sum of its inputs (not accounting for insertion losses). Thus the output varies in amplitude according to the state of the digital input. The dynamic range of the attenuator is adjusted by setting the signal level of the RF DAC range. A programmable phase shifter is similarly constructed using a 90° combiner in place of the 0° combiner in the programmable attenuator. The range of phase shift is set by adjusting the signal level of the RFDAC range.

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[1]U.S. patents pending (07/952,065, 08/055314).

[2]D. Hopkins, D. Yu, et al., Proc. IEEE Part. Acc. Conf., San Francisco, May 6-9, 1991, pp.1335-1337.

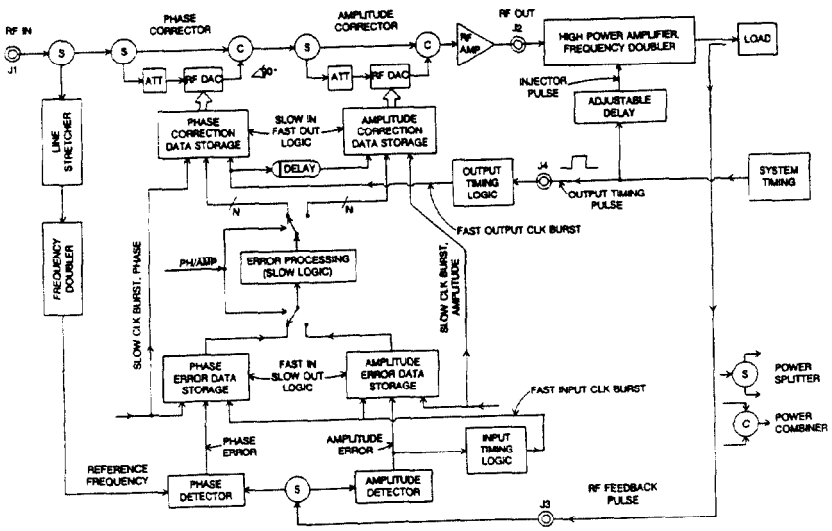

Figure 1 System Functional Block Diagram

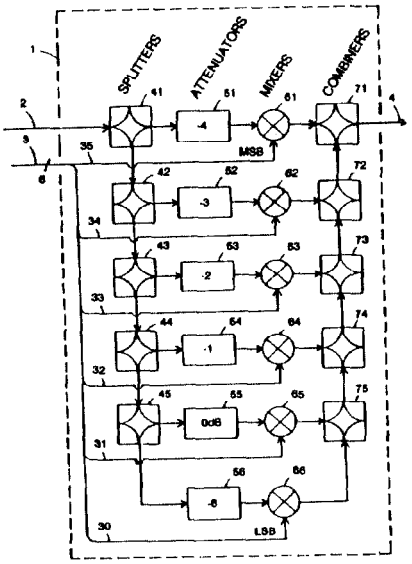

Figure 3 6-Bit RFDAC Schematic

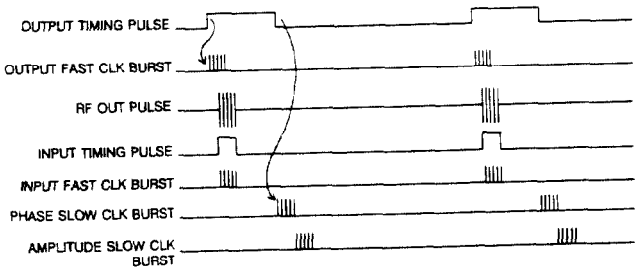

Figure 2 System Timing Pulses

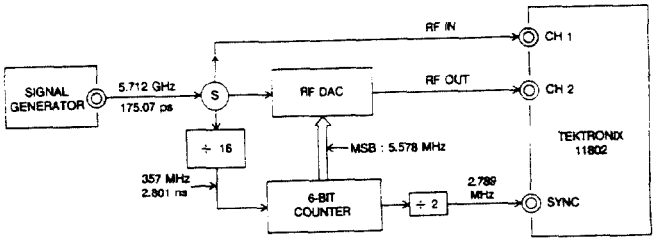

Figure 4
Dynamic Test Setup for an RFDAC Breadboard

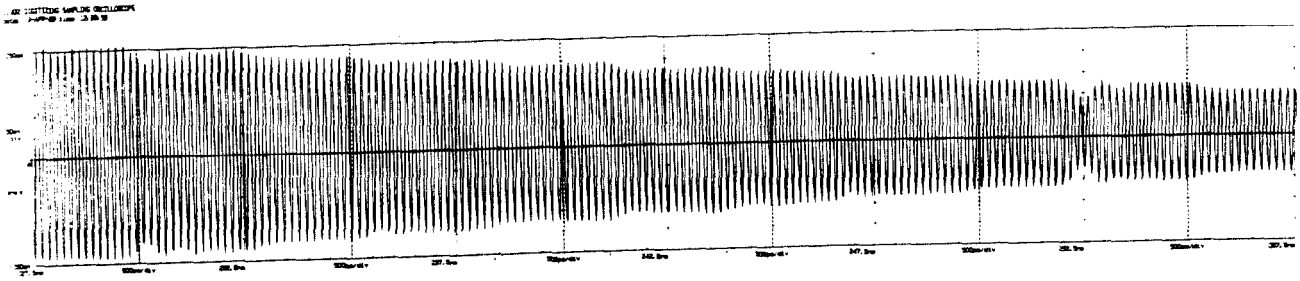

Figure 5 Staircase Test Results, 227.5 ns to 257.5 ns, in 2.8 ns Steps

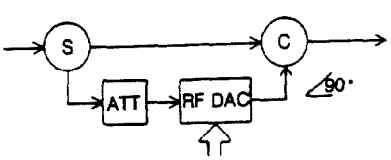

Figure 6 Programmable Phase Shifter/Attenuator