A Digital Beam Phase Loop for the Low Energy Booster

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Abstract

The Direct Digital Synthesizers (DDS) have a proven record of high frequency stability in accelerator beam control. For the Low Energy Booster working in the frequency range of 47MHz to 60MHz, a highly stable, high resolution DDS can improve the longitudinal beam stabilities. With the DDS as the source it would be highly desirable to make the beam phase loop digital. In this paper we show the description of the loop hardware and a method to simulate the performance in the presence of loop delay using a control system simulation software called SIMULINK. Some experimental hardware based on DDS system which was used to accelerate the beam in the FNAL booster is discussed.

I. INTRODUCTION

Reason for going to digital as compared to analog in implementing phase loop is due to (1) the advent of super stable, high speed and high resolution direct frequency synthesizers and (2) the opening of new opportunities to implement complete real time processor control without additional hardware modifications.

A. Frequency source

For the Low Energy Booster the accelerating frequency is varying through the cycle from 47MHz to 60MHz and there are tough requirements to both frequency stability and spectral purity of the source. The rate at which the frequency varies is considerably high (2.5GHz/s). All this is within easy reach with the Gallium Arsenide technology. Using conventional analog circuits the super frequency stability is hard to satisfy. Recently developed high-speed Direct Digital Synthesizers are very promising as master oscillators. Such a device being completely digital, except for an output DAC, provides 32-bit (2×10^{-10}) frequency resolution with its stability completely defined by external fixed frequency oscillator. Off-the-shelf ready to use synthesizers have stability to the order of 10^{-8} or better. However, the spectral purity depends on the clock frequency and the operating frequency. The output signal is generated by the digital adder - phase integrator, and hence there are no reasons for phase discontinuity unless the digital circuit is malfunctioning. The main concern will be about the phase/frequency noise, creating sidebands with the synchrotron frequency and its harmonics near the fundamental and other harmonics of the revolution frequency. There was also the fear about sidebands, generated due to stepwise frequency control during the cycle. This was calculated analytically for the LEB and was shown to be below -55dBc for a time step of 1.9μs so that all the dangerous components were insignificant.

B. Beam phase loop.

Even a perfect frequency source requires feedback in order to provide damping of dipole synchrotron oscillations. The block-diagram of phase loop together with the frequency source is shown in Fig. 1.

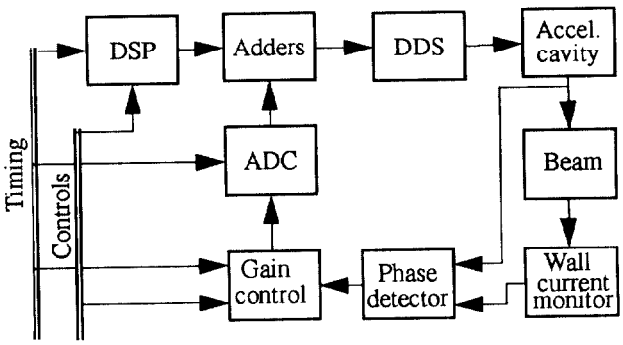

Fig. 1: Beam Phase Feedback Loop

In order to simplify the picture, radial position and synchronization loops are not shown. Digital signal processor (DSP) is used to provide the frequency profile, which is stored in its memory and the data is applied to the adder input with a rate of 500 kwords/s. A frequency down conversion based phase detector uses an intermediate frequency of 10.7MHz. The overall bandwidth is 300 kHz and linear angle range is ±150°. Gain control allows programmable loop gain during the acceleration cycle. The ADC is 10Ms/s with 12 bit resolution. Its speed is an essential parameter, since it defines the effective delay and contributes to the overall loop performance. Fast digital adder circuits are needed to close the phase loop.

The basic requirement for the phase loop is associated with damping of the coherent dipole oscillations. To meet this general requirement effectively the open loop gain of the loop has to be designed more than 2 at the highest synchrotron frequency[1]. For synchrotron frequency f_s and phase stability margin of 45° the limit of the total delay is: $t_{max} = 1/16f_s$, which gives 2.5μs and 2.1μs for the LEB and FNAL booster accordingly. This limitation becomes more tight if one will take into account phase shifts due to limited bandwidth of various parts of the loop, in particular - the phase detector and accelerating cavities. If we take into account the inevitable cable delays (0.5 - 1.5 μs), the feasibility of digital signal processing for FNAL

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booster becomes questionable. To proceed with this we started some experimental test on FNAL booster and also analytical and numerical investigation using SIMULINK/MATLAB software.

II. SIMULATION USING MATLAB SOFTWARE

In order to evaluate the loop performance in actual working conditions we have to build the complete hardware and then test with beam in the machine in the presence of other low level rf loops. On the other hand, if all the loops are decoupled, then the interaction between them is negligible. This allows us to independently design and simulate the loop by representing the hardware components as blocks with appropriate transfer functions. SIMULINK[1] is a good software package for modelling and simulating such control loops which is available in MATLAB. This software provides tools to investigate the behavior of nonlinear systems as well as systems with time varying parameters. The latter is particularly important for fast cycling boosters, where typical time of parameter variation is comparable with the period of the synchrotron frequency. Using SIMULINK it becomes easy to investigate the single particle behavior with a well known control terminology.

The loop is described using the set of standard as well as user-defined blocks (Fig. 2) and user-written command files. Fig. 3 shows the closed-loop frequency response of the phase loop for the LEB parameters with an effective delay of 1μs. Fig. 4 shows the response of the same loop to the phase step for three different values of the loop gains. For the open loop gain at the synchrotron frequency equal to 3.0 the damping is insufficient (Fig. 4). While decreasing the gain lead to reduced oscillatory response on the natural frequency as shown in Fig. 5 for a gain of 0.5. In Fig. 6 the step response for the optimal gain of 1.5 is shown.

Further steps in the simulation could involve time varying parameters, which will increase the permissible delay. Both radial and synchronization loops can be added to investigate their interactions with beam. Beam-loading effects are also easy to simulate.

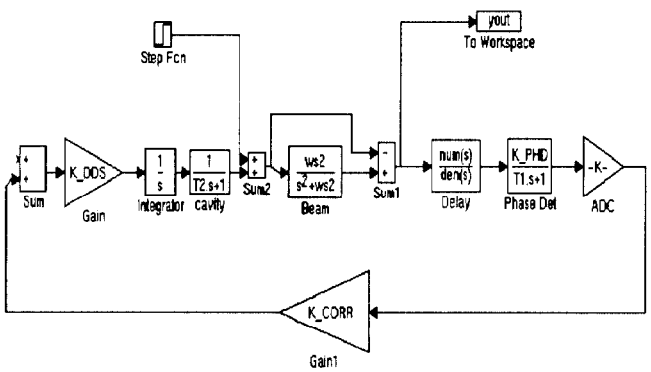

Fig. 2: SIMULINK model of the digital beam phase loop

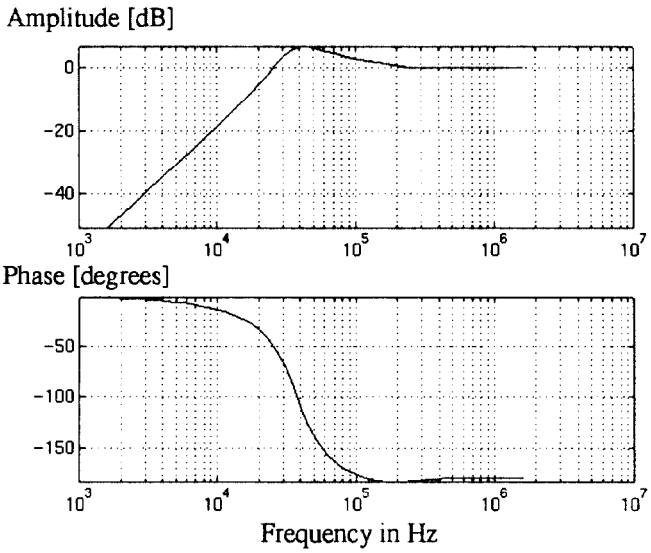

Fig. 3: Closed loop frequency response

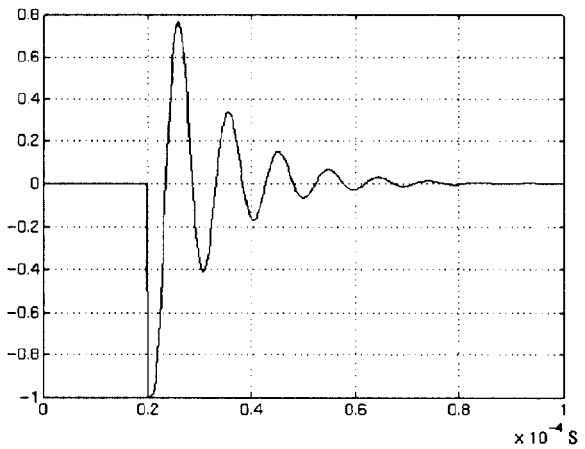

Fig. 4: Step response for G_s = 3.0

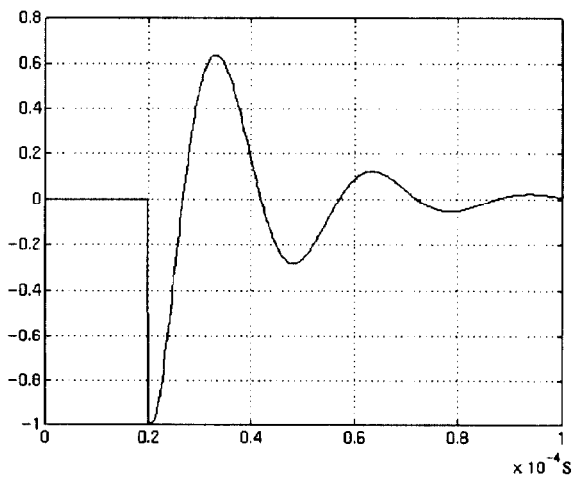

Fig. 5: Step response for G_s = 0.5

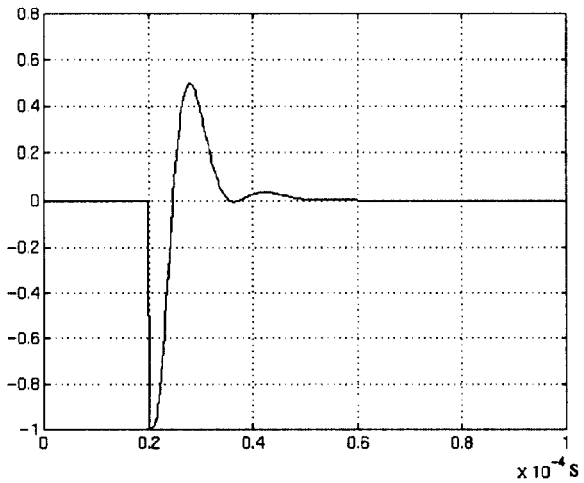

Fig. 6: Step response for G_s = 1.5

III EXPERIMENTAL STUDIES

Some experimental work on FNAL booster low level rf system was done to establish the feasibility of the Direct Digital Synthesizer based digital beam phase loop for a fast cycling machine. As a first step, which didn't require special beam time, the PLL loop, shown in Fig.7 for locking the DDS to the beam was assembled and investigated. Note that a cable delay of 1.4μs was introduced in the loop. The DDS was locked to the beam throughout the acceleration cycle with the phase error controlled to within 10°. The loop performance was completely defined by the effective loop delay and the processing algorithm in DSP#2. Digital processing time in DSP#2 contributed additional 1.2μs delay in the loop.

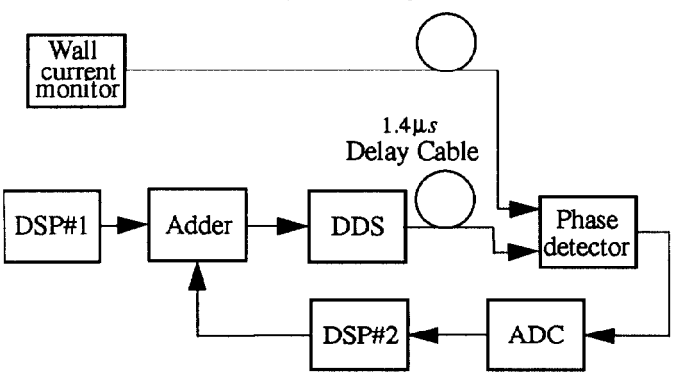

Figure 7. Experimental setup used at Fermilab

The second stage of the experiment was done by replacing existing VCO and part of the phase loop by the circuit shown in Fig. 7 with the exception of DSP#2. The DDS was made to drive the booster cavities to control the beam in the ring. After setting appropriate loop gain the acceleration was immediately obtained. All the qualities of the beam expected from a normal booster run was preserved during the operation with the DDS. The experiment was conducted upto full booster intensity. The accuracy of the DDS/DSP frequency profile was, as it was expected, significantly better than that of the VCO. The delay contributed by the ADC, adder circuits and the DDS was about 0.6μs. This was the first and complete proof of a digital frequency source together with partly digital phase loop which worked on an existing fast cycling machine. With this experience we believe that there are good opportunities which lie ahead to use the hardware for the LEB so that the reliability and the quality of beam can be greatly improved.

IV. CONCLUSIONS

Control systems-oriented SIMULINK software is a useful tool for the analysis of beam-control systems with time-varying parameters. Using SIMULINK a simple way of modelling and then the simulation of the practical digital beam phase loop is shown. Direct Digital Synthesizer has proved to be a precise RF source for the frequency range of 30MHz to 60 MHz and with a df/dt ≈ 3GHz/s. So it can be used for the LEB as well as for the MEB and the HEB. As the time progress we can expect further growth in DDS technology which will allow us to use it at 360MHz for the collider.The possibility of using Digital Signal Processors in fast-cycling booster phase loop is limited by the loop time delay. LEB has a good layout of the RF cavities, wall current monitor and low-level RF equipment. So, the existing TMS320C40 DSP could be used while delay budget in the FNAL booster barely allows such things. Having a DSP directly in the phase loop as in Fig. 7 is useful to introduce active and passive filters with time-varying gains. Evidently, for larger and/or slower machines a complete digital RF sources and the feedback is an advantage.

V. REFERENCES

1. H.G. Hereward, "Open and Closed Loop Properties of an RF Accelerated Beam", CERN/PS/4497, 1960.
2. SIMULINK User's Guide, The MathWorks, Inc., Massachusetts, March 1992.