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# A Prototype BPM Electronics Module for RHIC*

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*Abstract*

Prototype components of the VXI-based Beam Position Monitor Electronics for the Relativistic Heavy Ion Collider have been constructed and tested for accuracy, resolution and linearity. The detector, designed solely for single-bunch acquisition, consists of a homodyne detector followed by a sample and hold and Analog-to-Digital Converter. In the final modules, an on-board Digital Signal Processor will provide turn by turn data correction, continuously updated closed-orbit averaging, and circular buffer maintenance. A timing processor allows synchronization of modules to enable correlated data collection.

frequency (78 kHz) and digitally calculated closed orbit at the synchrotron frequency (less than a few hundred Hz). The design philosophy is to digitize as soon as possible in the processing chain, perform all data correction and position calculation digitally within the module itself, and store results in on-board memory. A Digital Signal Processor is being designed into the BPM electronics module for this purpose.

All RHIC BPM electronics modules will conform to the VXI (VME Extension for Instrumentation) specification for register based C-size modules. All memory will be directly mapped into the VXI memory address space, allowing stored data to be accessed at high speeds.

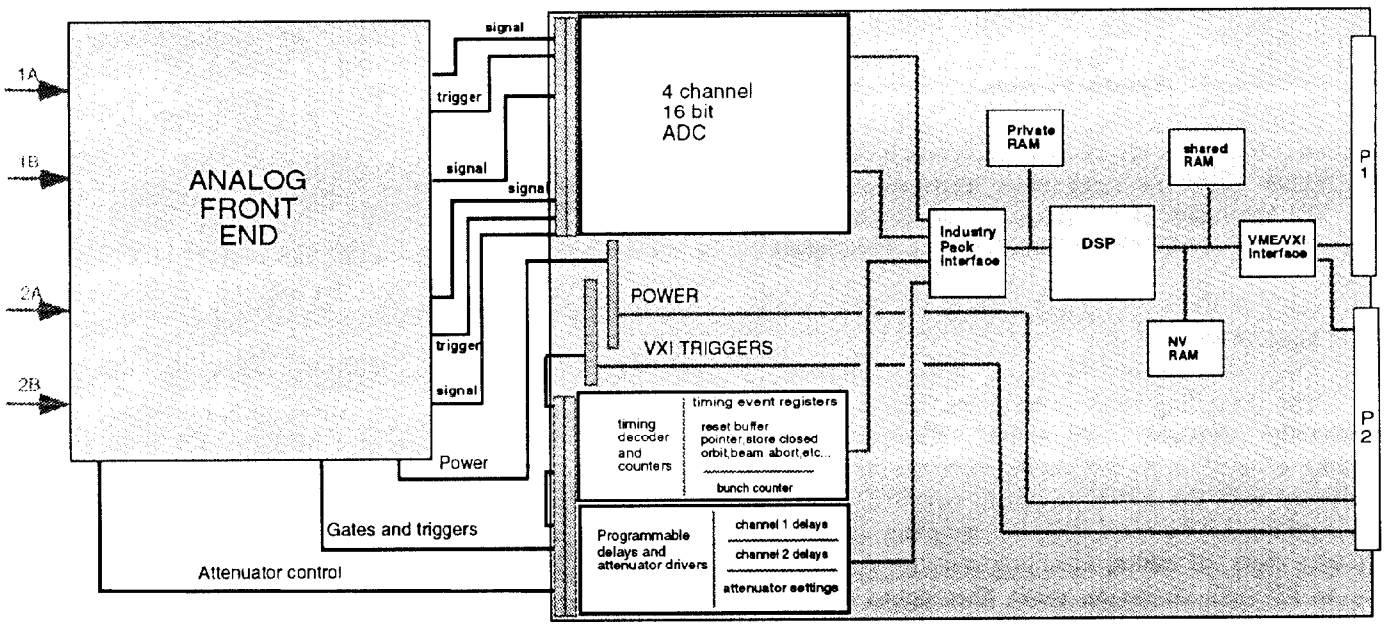


**Figure 1. Block diagram of the position monitor electronics module**

## I. Introduction

As previously described[1], the RHIC position monitor system will contain over 500 BPMs in the two storage rings and over 40 BPMs in the injection lines. Most monitors in the injection lines and regular arcs will measure in only in the plane of maximum beta. Others will measure in both planes. All monitors share a similar design based on shorted 50Ω striplines approximately 23 cm long[2].

The RHIC BPM electronics are being designed to simultaneously provide single bunch acquisition at the revolution

As seen in Figure 1, the BPM electronics is being developed in two parts: the analog front end, which consists of a pulse detector mounted in the front half of the VXI module, and the digital acquisition section, which consists of the DSP-based VXI card with daughterboards containing the digitizers and timing interface circuitry. The analog front end has been through several prototypes with test results from the latest version reported here. The DSP and VXI interface design is being done in cooperation with the Brookhaven Instrumentation Division and first prototypes are due during the summer of 1993. Digitizer prototypes are under construction and the timing circuitry is currently being tested.

* Work supported by the U.S. Department of Energy



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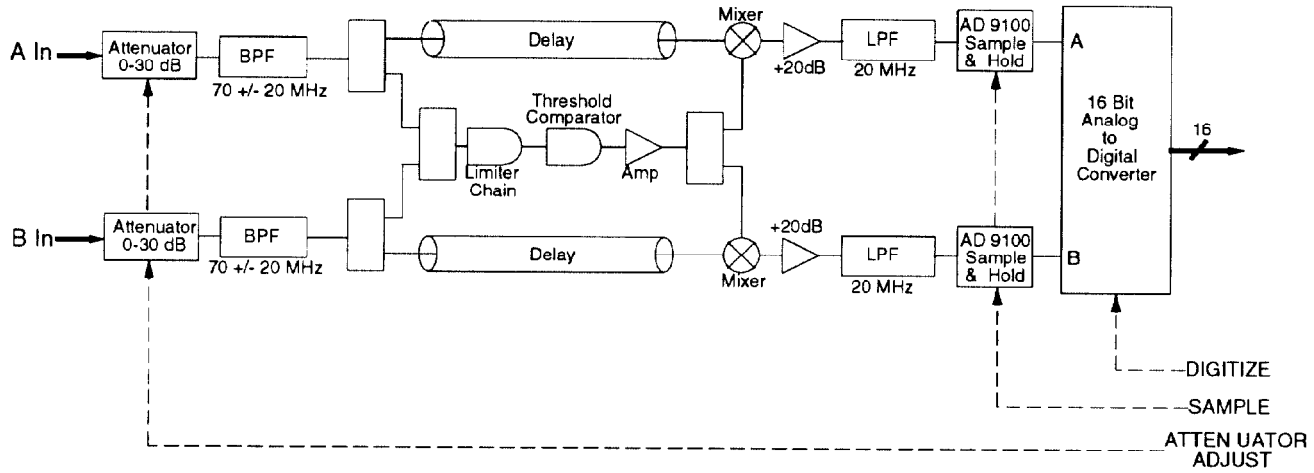


**Figure 2. Block diagram of the synchronous detector prototype**

## II. Analog Front End

### A. *Beam characteristics*

RHIC will contain relativistic beams of ions in the mass range from protons through fully ionized gold. The bunches will be accelerated in a 26.7 MHz accelerating RF system, and undergo a bunch rotation at top energy to allow clean transfer to a 196 MHz storage RF system. All ions except protons will pass through transition. Minimum bunch spacing is 110 ns with a single gap a few hundred ns long to accommodate for the extraction kicker risetime.

**Table 1: Dynamic range requirements**

| Parameter | Min | Max | Effect on Common Mode Power |
|---|---|---|---|
| Intensity | $10^{10}$ e/bunch | $3x10^{11}$ e/bunch | 30 dB |
| Bunch Length | 1.2 m | 5.1 m | 9.5 dB |
| Position | -20 mm | +20 mm | 7.5 dB |
| | -5 mm | +5 mm | 4 dB |

By using these beam characteristics in a system simulation[3], the dynamic range required of the analog front end can be determined. A useful subset of the simulation results is shown in Table 1. For a fixed intensity, the full dynamic range of common mode power (total power transmitted through the two BPM cables) due to changes in beam position and bunch length is 17dB. This is the absolute minimum instantaneous dynamic range required of the analog front end, but for operational convenience much more will be provided.

### B. *Analog front end specifications*

The following points summarize the specifications and design philosophy of the analog front end:

1. Single bunch acquisition.
2. Maximum bunch acquisition rate: 78 kHz (the revolution frequency).
3. Position uncertainty at center for entire system (BPM + electronics): <0.13mm.
4. Single bunch resolution for commissioning (single bunch, $10^{10}$ protons per bunch): <1mm.
   For operating storage (>$10^{11}$ protons per bunch, or $10^9$ gold ions per bunch): <<0.1mm
5. Bunch-to-bunch coupling: < -60dB
6. Instantaneous Dynamic Range: >17dB.
   Programmable attenuation: >30dB.

### C. *Analog Front End Prototype*

The analog front end, shown in Figure 2, is a homodyne detector optimized for single bunch acquisition, using bandpass filters on the input for pulse stretching, and adjustable attenuation for increased dynamic range. The bandpass filter has a 40MHz bandwidth, very wide for this type of application, which is necessary to keep the bunch-to-bunch coupling less that -60dB with the 8.9MHz bunching frequency. Due to the large amounts of power coupled through 40MHz bandwidth, 30dB of adjustable attenuation can be used to increase the dynamic range of the detector. The homodyne detector itself combines a limiter chain with a comparator threshold detector to generate the mixer LO signal. This arrangement gives >50dB dynamic range while preventing oscillations in the detector loop. This is a necessity for single bunch acquisition, where a continuous signal and its ability to overcome loop oscillations does not exist.

One of the design goals for the analog front end was to make sure that the noise signal input to the S/H and digitizer was the same or slightly larger than the digitization output

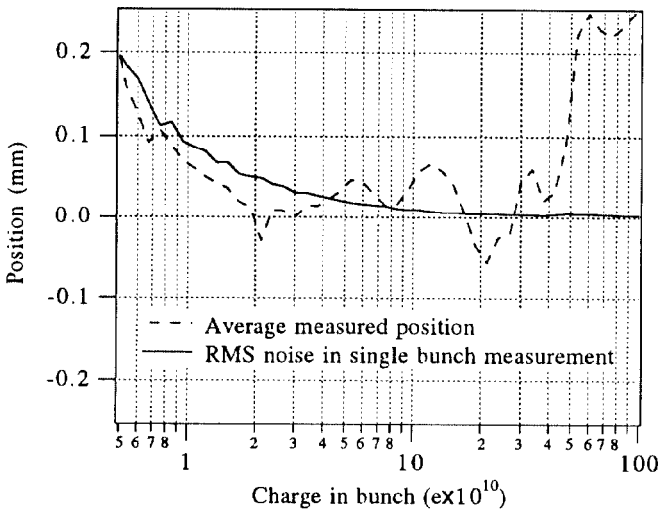


**Figure 3. Single bunch performance**

noise seen with a 50Ω termination on the S/H input. This insures that the maximum signal to noise ratio is being achieved. Even with a 20dB gain block after the detector, this criterion is maintained.

The signal is then sampled with an AD9100 monolithic sample and hold, and for these bench tests only, it is digitized with a ICS-140 VME card, which uses two Crystal CS5101 16-bit digitizers for simultaneous acquisition. In the final implementation, the 16 bit ADCs will reside on a daughter card on the digital acquisition board. Results of single bunch bench tests are shown in Figure 3. For these tests, a bunch under storage conditions was simulated and a 20 dB input attenuator was used. For low intensity operation, the 20 dB attenuation would be switched out and similar performance would the be expected for bunches with an order of magnitude less charge. Performance of the front end prototype under both CW and single bunch conditions is summarized in Table 2. The

**Table 2: Performance of Prototype Front End**

| | 70 MHz CW Detection | Single Bunch Detection |
|---|---|---|
| Accuracy | +/- 50μm | +/- 50μm |
| Dynamic Range | 50dB | 30dB |
| Resolution | <10μm RMS (40MHz BW) | <20μm RMS |

dynamic range quoted is the instantaneous range for the given accuracy and does not take into account the availability of variable input attenuation. The immediate design goal is to increase the operating dynamic range for single bunch acquisition to approach that of CW operation. To achieve this, all components of the detector must be matched for transient operation.

## III. Digital Acquisition Section

Table 3 summarizes the functionality of the digital acquisition section shown in Figure 1. The RAM (used mostly for the buffers), DSP, VXI interface, and Industry Pack (IP) interface are all provided on a board within the C-size module. Space for four industry packs is provided in each module and the ADCs and timing decoder reside on these IPs. Using IPs for the more specific circuit functions allows the same DSP board to be adapted for different applications, avoiding inefficient design reproduction.

**Table 3: Specification of the digital acquisition section**

| Feature | Specification |
|---|---|
| closed orbit buffer | 10 second deep circular buffer; initialized, updated on globally distributed timing events, and stopped on abort event |
| turn by turn buffer | several synchrotron periods deep; initialized on a timing event and updated on a trigger locally delayed from a turn-by-turn event |
| timing decoder | decodes several timing events; counters provide synchronization with any bunch and programmable delay lines provide 2ns resolution |
| DSP software | perform within a single turn (12μs): acquire 4 digitized values, apply corrections, calculate position & charge, average closed orbit, and update buffers |

## IV. Calibration system

In-place calibration will be provided to test the electronics from the control room, as the hardware cannot be accessed while the machine is in operation. The calibration input to the BPM processing chain is a stripline directional coupler attached to the cryostat. This will couple a calibration signal, a simulated beam pulse generated in the equipment alcove, equally to both inputs of a BPM channel. Variation of the input attenuators will permit both offset and gain calibration. By injecting the pulses into the directional coupler during the extraction gap in the beam, calibration measurements can be made during machine operation.

## V. References

[1] T. J. Shea, Design Studies on the RHIC Position Monitor System, BNL-48048, AD/RHIC-114, 1992.

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[3] W. A. Ryan and T. J. Shea, An Interactive Beam Position Monitor System Simulator, Workshop on Accelerator Instrumentation, Berkeley, October 1992