HIGH DENSITY DATA RECORDING FOR SSCL LINAC

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Abstract

The Superconducting Super Collider Laboratory and AlliedSignal Aerospace have collaboratively developed a high density data monitoring system for beam diagnostic activities. The 128 channel data system is based on a custom multi-channel high speed digitizer card for the VXI bus. The card is referred to as a Modular Input VXI (MIX) digitizer. Multiple MIX cards are used in the complete system to achieve the necessary high channel density requirements. Each MIX digitizer card also contains programmable signal conditioning, and enough local memory to complete an entire beam scan without assistance from the host processor.

I. BACKGROUND

A compact 128 channel data system was needed for performing beam diagnostic activities. To accurately profile the expected beam pulse, the 128 channels would have to be sampled simultaneously every 50 nSec for a period of up to 50 uSec. There was not anything commercially available that could perform this function within the allocated 24" rack space. In addition to the high number of channels to be digitized, the incoming current signals had to be converted to a voltage and amplified to the proper level before being recorded. Manufacturing costs and development time of the system were also considered important due to schedule and cost constraints. The time allocated for development and manufacture of the first board was targeted at 16 weeks.

II. EARLY DEVELOPMENT

Preliminary design and layout activities revealed that eight 20 MHz channels of data per VXI board was the practical limit. Higher levels of integration could yield slightly higher channel counts, but the increase in development time and cost would become significant. Even in the eight channel board layout, very little room remained for signal conditioning. At this point we decided to split the board functions between generic digitizing functions and signal conditioning functions. The entire main board or 'motherboard' would contain the 8-channel digitizing functions and the control interface. The 'daughterboards' were then assigned the exclusive tasks of signal conditioning. There is just enough room inside a VXI module to allow the daughterboards to be stacked on top of motherboard.

III. MOTHERBOARD DESIGN

Digitizing

The motherboard consists of eight independent channels. Each channel has its own flash converter and 256K memory (128K samples). The flash converters are 10-bit, 20 MSPS devices that were selected for their power-consumption, performance and cost parameters. The memory is high-speed CMOS static RAM using 128K x 8 chips. A Programmable Logic Device (PLD) is used to control data acquisition, triggering and timing for all eight channels.

Timing

The PLD controls the timing and memory usage on the board. To optimize the memory for performing beam scans, the memory is divided into 100 records of 1K each. After the board is armed, each trigger pulse initiates a 1024 point digitized record covering 50 uSec. After the record is complete, the card remains armed and ready for the next trigger. After trigger pulse number 100, the card will automatically disarm and ignore further trigger pulses. If fewer than 100 pulses are desired, a starting record other than zero may be pre-loaded into the current record counter. For example, loading a 99 into the current record counter would allow only one record to be taken before disarming.

The PLD may be put into an alternate single shot trigger mode. This mode effectively makes each record one sample long. Since each trigger pulse takes only one reading (instead of 1024), then 102,400 individual readings can be taken. The PLD used is an electrically erasable Altera 7032 device in an on board socket. It can be easily removed and reprogrammed for different memory or timing configurations.

Clock and Trigger Modes

To give the board maximum flexibility for use in multiple board systems, several clock and trigger options are available. The clock may be jumper selected from one of three sources; 1) A front input clock connector, 2) an on board 20 MHz crystal oscillator, or 3) the clock may be taken

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off the VXI local bus. Option 3 is provided so that multiple cards on a VXI backplane can be synchronized with the first card in the series.

The trigger to initiate a data record can also be jumper selected from a number of different sources. Again the VXI local bus or VXI trigger bus can be used as a trigger source.

Daughterboard Interface

The motherboard also provides the necessary interface signals, power, and connectors to the daughterboards. Each channel on the daughterboard is individually programmable. The following signals are provided for each channel on the daughterboards through the interface connector;

1. +5, -5, +12, -12, GND power.
2. Four digital control lines.
3. One 12-bit DAC voltage (-1 to +1).
4. Differential input from front panel.
5. Differential output to A/D converters.
6. Differential calibration input from front panel.

VXI Interface

The simple VXI register based interface is used for all board control and data transfer operations. The interface chip and design were purchased from Hewlett Packard as part number Z2492A. The data from the eight channel local memory bus are mapped to eight registers in the VXI A16 address space. The local address pointer can be loaded and incremented through a control register. All the data is then read across the VXI bus by reading all eight channels and then incrementing the local address pointer.

The register based interface was selected over a message based interface because of the higher transfer rate. Further improvements to the transfer rate could occur if the local memory could be mapped directly into the VXI A32 address space. This was not done on this design due to the delivery time and development cost constraints.

IV. DAUGHTERBOARD DESIGN

Requirements

The eight channel motherboard is designed to accept four daughterboards, with two channels on each board. The function of the daughterboard is to convert low level current signals into the ± .5 volt signal for the motherboard. To cover the expected range of values, the amplifier supplies a full scale output (± .5) for inputs of 10 μAmps to 10 mAmps. The amplifier also needs to have a high enough frequency response to follow an input rise-time down to 100 nSec. These electrical parameters have to fit within the size allowed by the enclosure, and use only the power and signals supplied by the motherboard.

Amplifier Design

In order to maximize the resolution of the 10-bit A/D converter, the amplifier has to have enough ranges to keep the maximum signal level in the upper part of the A/D range. The higher the signal can be to full scale, the greater the resolution. A two stage amplifier was designed to handle these requirements.

Stage one of the amplifier is a differential current to voltage (I>V) converter that covers three decades. The three ranges of one decade each, are achieved by switching different scaling resistors into the feedback of the I>V stage. A relay is also included on the daughterboard so that a calibration signal can be routed directly to each amplifier. All the relays are controlled by the four digital control bits provided for each channel.

The second stage of the amplifier contains a voltage programmable amplifier. The gain can be varied from 1 to 10 using the ± 1.0 volt DAC voltage from the motherboard. This effectively yields a continuously variable I>V converter over the entire three decade range. This does not occur without some sacrifices.

The second stage does not have a consistent voltage vs gain curve from channel to channel. This requires that each channel have some calibration factors that are determined during calibration. In addition to the gain variations, there is a large offset at the amplifier output. The offset is consistent at a particular gain setting, but varies as the gain is changed. The good thing is that both of these undesirable characteristics are repeatable. To handle this in our checkout software, we selected nine discreet gain settings for the second stage. For each gain, the DAC value for the proper gain and an OFFSET value are stored. These are determined through application of a DC calibration signal and stored on a disk file. During data collection, when a gain range is selected, the exact DAC value for that channel and gain is written to the motherboard DAC for that channel. When the data is read in, the OFFSET value is added to the data so that it is corrected. This was all performed within some low level device drivers written in C. Once the driver routines were completed, this manipulation became invisible to the application program. By using a programmable voltage source, software was written that determined the two calibration factors for each of 25 selected gain settings. Because of the calibration relays on the daughterboard, the calibration process is completely automated and takes about one minute for an 8-channel system.

V. SUMMARY

The motherboard serves as a general purpose eight channel 20 MSPS digitizer. By adding a different daughterboard design, an entirely different set of inputs can be digitized. The daughterboard is easily changeable and can be as simple as a jumper wire, if the input signal is already in the ± .5 volt range.

The daughterboard is a continuously variable gain I>V converter that can supply a full scale input to the motherboard for any current input from 10 μAmp to 10 mAmp.

Multiple 8-channel MIX digitizer modules can provide up to 96 channels of 20 MSPS current monitoring in a single VXI rack. Using two VXI racks, the 128 channel beam monitoring system was accomplished with eight empty VXI slots available for additional instrumentation.

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