Collider Bypass Diode Thermal Simulations and Measurements for the SSCL*

Cyrous Rostamzadeh and Gerry Tool
Superconducting Super Collider Laboratory
2550 Beckleymeade Avenue, Dallas, TX 75237-3997 USA

Abstract

Warm bypass diodes will be used as a component of a quench protection system to bypass an exponentially decaying current of 36 sec. time constant and peak current of 7000 A. Temperature excursions due to approximately 252 Kilo Ampere Sec. are studied using ANSYS, a finite element analysis program. A parabolic current waveform of similar energy but higher MIITs (1058 MIIT) was applied to the bypass circuit and temperature excursion was measured at various locations. The procedure of current waveform generation and thermal measurements is illustrated in this paper. A comparison of simulation technique with actual measurements confirms the accuracy of the bypass diode assembly model. This assembly is installed at the SSC half-cell string test facility and results are extremely encouraging.

I. Introduction

A design has been created, and thermal analyses of the assembly performance have been conducted to predict the temperature rise in the assemblies during the current bypass function. The purpose of these tests is to verify with physical measurements that the assembly design is adequate, and to gauge the accuracy of the thermal analysis procedures for future use.

Figure 1 shows the electrical circuit of Accelerator System String Test (June 1992) in which these assemblies are connected. The nominal bypass current waveform to be conducted by the bypass assembly during quench is shown in Figure 2. The test setup used was not easily configured to provide an exponential decay from an initial value, so a power supply was programmed to provide a fast rising current to I_0 followed by a parabolic decay as shown in Figure 3. The waveform was configured to provide the same $\int Idt$ as that to be exercised during the operational scenario. The nominal peak operating current for the collider is 6500 A, but a special "conditioning" scenario possibly requires operation at 7000 A. Therefore, our tests exercised the devices to this level.

II. Test Setup Description

Each bypass diode assembly consists of two independent (thermal and electrical) diode circuits which can be configured as one, two, or three diodes in series. Each of these independent circuits can be used to protect one or more magnets which together make up a "quench bypass unit". Figure 4 shows a total assembly loaded with 3 diodes in each section. These tests were conducted using a three-diode and a two-diode stack.

Each circuit is composed of a stack of International Rectifier type R77R6A diodes alternating with copper disks acting as heat sinks and clamped under a force of 10000 lb. Disks next to the anode side of the first diode and the cathode side of the last diode are connected externally through copper bus bars (3/4" x 1/2") brazed to the copper disks. A pair of MCM500 bypass cables is connected to each of the bus bars using two-hole MCM500 lugs.

* This work supported by the United States Department of Energy under contract DE-AC35-89ER40486.

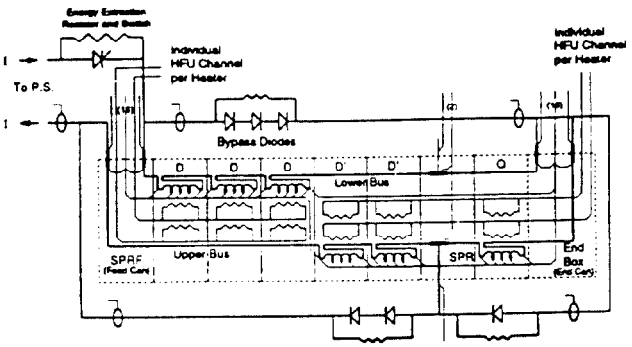

Figure 1 - ASST Phase I Electrical Circuit

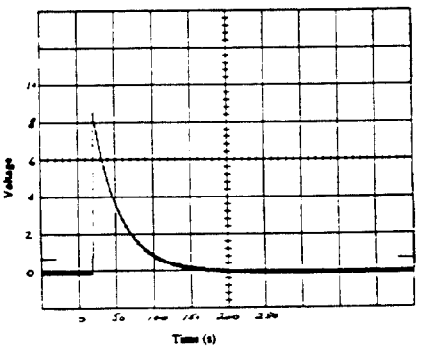

Figure 2 - Nominal 7 kA Program to power supply (10V = 8000A)

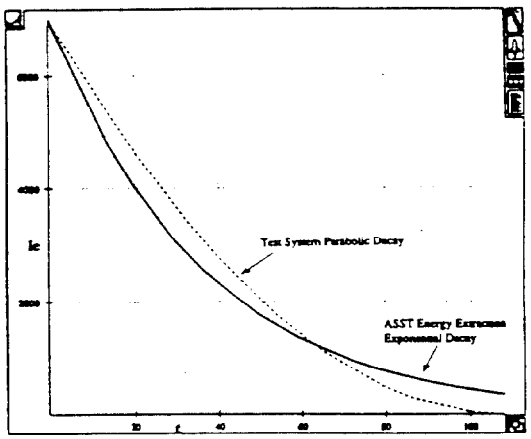

Figure 3 - Parabolic Approximation to Nominal Current Waveform

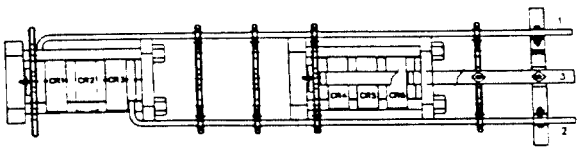

Figure 4 - Assembly with 3 diodes in Series

Thermal sensors (RTD - Resistor Temperature Detectors) were inserted into the sides of the copper disks between the diodes and in the connecting bus bars to monitor temperature excursions during current pulsing. Instrumentation cables were used to interface the RTD signals to signal conditioning amplifiers (OMEGA OM3-600). Signals were digitized and stored in two Lecroy data loggers for analysis. Sampling rates of 1 Hz and 10 Hz were used to record slow and fast processes. Table 1 lists the signals measured and the data logger channels for the first series of tests using one 3-diode section

Table 1: Data Logger Signal Definitions

Description	Calibration	Lecroy 1 Signal Name	Lecroy 2 Signal Name
Anode 1 Bus	200°C/10 V	V8	V4
Anode 1	600°C/10 V	V10	V5
Cathode 1	600°C/10 V	V11	V6
Anode 2	600°C/10 V	V12	V7
Cathode 2	600°C/10 V	V13	V8
Cathode 3 Bus 2 (3/4")	200°C/10 V	V6	V2
Cathode 3 Bus 1 (18")	200°C/10 V	V5	V1
LEM Transductor	10 kA/5 V	V9	V14

The bypass diode assembly was inserted in a 4 ft long G10 sleeve for 3.5 kV dc electrical isolation from ground. The total assembly was then inserted into a 4 ft long stainless steel tube similar to the enclosure that will be used for mounting the assemblies in the eventual Collider tunnel.

A 0.1% LEM transductor was used to monitor the bypass current waveform. The actual accuracy of this device was less than specification due to use of an uncalibrated burden resistor in this setup, therefore, a comparison was made with the IRING current transductor measurement in the power supply. the comparison indicates approximately 1% difference between the two signals in the $\int Idt$ for the current pulses used. The signal from the LEM transducer was instrumented by an Analog Devices amplifier (3B41) before connection to the data logger for digitization and storage. The String Test power supply control microprocessor (SECAR) was used to generate a parabolic waveform that is comparable to the real waveform as discussed earlier. This waveform provides the current reference for a Dynapower power supply capable of delivering 0 - 8000 A at 0 - 40 V.

The diode assembly was connected across the power supply in various configurations:

1. three diodes in series,
2. two diodes in series,
3. five diodes in series.

We also added additional copper mass (disks) to the three diode configuration for later runs.

III. Test Process Description

The power source was easily programmed to provide parabolic and linear ramp segments. For a parabolic decay waveform to provide the same heating effect as the exponential decay, one wants to match the $\int Idt$ in the two waveforms since the voltage drop across diode devices is approximately constant in the current range of interest. (For a resistive system, such as the bypass cabling, the heating is proportional to the $\int I^2dt$. Analysis of the exponential and parabolic waveforms then leads to the condition that $I_0\tau = {}^1/_3 I_0 t_f$, where τ=36 s for the exponential decay and t_f is the final time at the end of the parabolic decay. This condition results in t_f=108 s for the case where $\int Idt$=252 kA-s. Since the resistive parts of the system will be heated proportional to $\int I^2dt$, we calculate that result for the maximum stress waveform and find that for the parabolic decay, $\int I^2dt$=1058 MIITs as compared with 882 MIITs for the reference exponential decay. This additional heating in the cables and connecting busbars is in a safe range and assures that we have data from a case which is more pessimistic than actual Collider operation.

A variety of electrical tests were performed and temperatures at the points listed in Table 1 were recorded. The power supply was quickly ramped up at 1.4 kA/sec starting from an initial current of 50 A and was then parabolically ramped down. On the first run with the three diode configuration, the peak current was limited to 3500 A, and the temperature profile was recorded. Six more runs were performed by increasing the peak current in 700 A steps. The waveform generation algorithm used easily scales the peak current with fixed rates of change, so the waveforms at different currents do not have areas which scale with the peak current value. Hence, data must be analyzed with respect to the actual waveform area, not with respect to peak current.

Tests were also performed on the two-diode section and on the two sections in series by strapping the two independent sets together. In order to establish that damage had not occurred during the high current testing, reverse bias measurements were made on all 5 diodes before and after electrical and thermal stress.

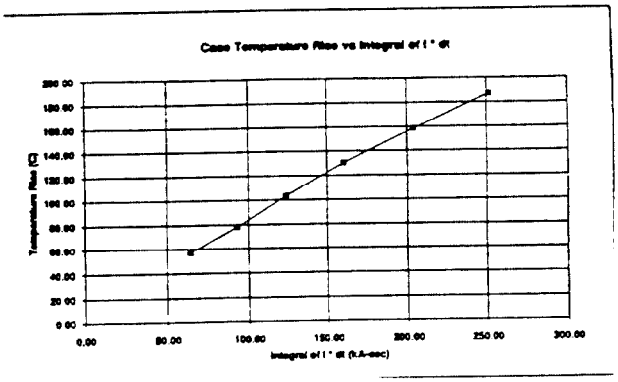

Figure 5 - Temperature Rise at Hottest Spot in Assembly

IV. Data Analysis

Data was extracted from the Lecroy data logger files on computer system, reconfigured to a convenient format, and plotted using the SPICE circuit analysis postprocessor tools.

Table 2 and Figure 5 indicate the temperature rise measured at the hottest spot in the assembly as a function of the area under the I vs t curve during these tests.

The current waveform and temperature profile vs time at four points along the assembly are shown for the 7000 A run in Figure 6 and Figure 7.

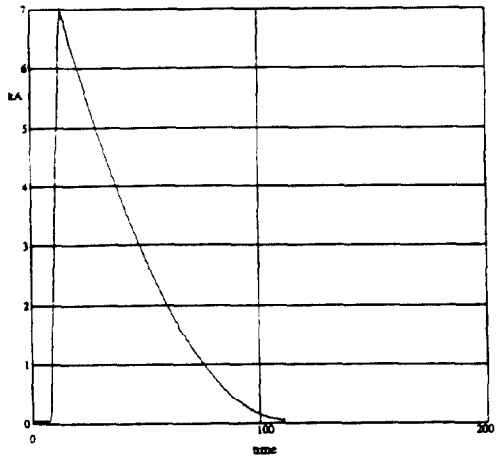

Figure 6 - Current Waveform for Test at 7 kA

Table 2: Temperature Rise during Experimental Rise

Run	Peak Current (A)	T initial (°C)	T Final (°C)	∫ Idt (kA-s)	ΔT (°C)
1	3,500	20	76.8	64.3	56.8
2	4,200	24	102.2	93	78.2
3	4,900	23.1	126.3	124	103.2
4	5,600	24.7	155.1	160.6	130.4
5	6,300	26	184.2	203.8	158.2
6	7,000	36.7	223.7	251.7	187

V. Comparison With Thermal Analysis

As indicated above, prior to the testing, a finite element model was constructed to perform a thermal transient analysis of the diode assembly using ANSYS. The purpose of the study was to predict the maximum temperature of the silicon wafers of the diodes and to provide a basis for comparisons of temperatures that could be measured and hence extrapolated to the silicon wafer.

The model placed three diodes in series as described in the test setup description. Details of the two-dimensional axisymmetric thermal solid modeling included the mechanical dimensions and thermal properties of the many different layers such as the copper cathode and anode, molybdenum buffer, silicon wafer, aluminum junction and silver disk. Details of the construction of the diode were provided by Art Felix of International Rectifier. The material properties were obtained from the CRC handbook.

The heat generation function applied to the silicon wafer layers was

$$P_d = 693.4\, e^{-t/36} \ln(1+7\times10^{14} e^{-t/36}).$$

Natural convection was assumed to occur to the bypass cables. The simulation results predicted a maximum temperature of about 233°C at the outside edge of the silicon wafer, with the peak occurring about 60 s after the heat generation started as shown in figure 8. The simulation results indicate a temperature profile very close to that measured in the tests.

VI. Thermal Recovery

During the test runs, the recovery to ambient temperature takes about 2 hours. In the operation of the Collider, this presents no problem since data analysis from the quench and recovery of the refrigeration system to operating conditions require a similar length of time.

VII. Conclusions

The tests have shown that the current design will work satisfactorily for the Collider with three or less diodes per bypass unit (number of diodes is dependent on bypass unit inductance and ramp rate). From separate measurements made in the laboratory, the forward conduction threshold of the three diodes is 0.95 V at 35°C, allowing a maximum ramp rate of 4.2 kA/s with magnet inductance of (3 x 75 mH = 225 mH) and for a leakage current of 1.5 mA established as the system requirement.

The peak temperature rise of the assembly is much higher than good design practice would allow for steady state operation such as in power converter applications. However, the transient, low rate of occurrence nature of this application coupled with the absence of reverse bias voltage for the device to block after the current pulse permits reliable operation of these diodes at temperatures above 250°C according to the manufacturer.

VIII. Acknowledgments

The tests described above were conducted with the cooperation and assistance of Al McInturff and Bob Flora of Fermilab, Milan Kuret, Roger Nehring, Gerry Sorensen and Nghia Tran of SSCL, and Art Felix of International Rectifier.

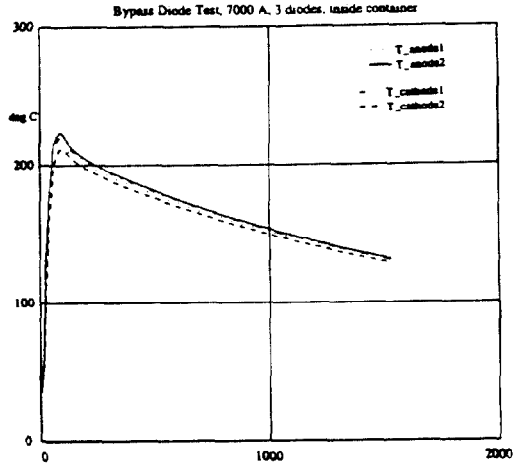

Figure 7 - Temperature Profile vs Time for 3-Diode Assembly at 7 kA

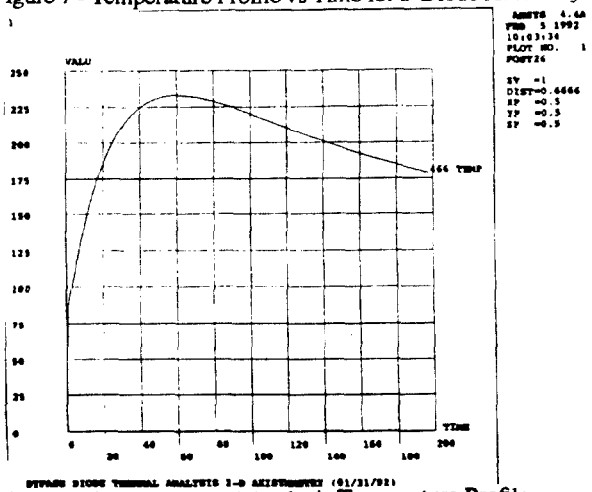

Figure 8 - Thermal Analysis Temperature Profile