A Pulse Sequencer for the KAON Factory Beam Chopper

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Abstract

The beam chopper consists of a low-loss transmission line center fed from a tetrode. The transmission line is terminated with a short-circuit at one end and an open-circuit deflector plate at the other end. The complex reflections from the open-circuited and short-circuited ends allow a single tetrode to generate a deflector pulse with good rise and fall times. The shape of the pulse at the deflector plate is extremely sensitive to the frequency of the grid driver pulse. A variation of 1ns in timing significantly alters the deflector pulse. To provide the required pulse pattern, a FET based grid pulser and sequencer has been built. This sequencer is able to produce alternating narrow and wide 900 volt grid pulses with rise and fall times of 20ns. Under computer supervision it is able to generate and control pulse patterns with a stability of ±125 ps. The pulse pattern is synchronized to an RF synthesizer to simulate operation with the 23 MHz TRIUMF cyclotron RF system.

I. INTRODUCTION

Kicker magnets will be required for ring-to-ring transfers in the KAON factory synchrotron at TRIUMF. The cylotron will be used as an injector for the synchrotron. To prevent beam spill at the transfer points, gaps must be introduced into the injected beam of sufficient duration to allow the kicker magnets to switch on and off. These gaps are produced using an electric kicker [1] operating at up to 15kV. This beam chopper is required to remove 2 and 3 beam bursts alternatively at approximately 1μs intervals.

Within the cyclotron the pulse period is 43.5ns. Each pulse has a width of 2.4ns with approximately 2.4ns of jitter. This results in an effective time between beam bursts of about 39ns. Therefore to remove two and three beam bursts the chopper pulses must be 48ns and 92ns alternatively with a rise and fall time of less than 39ns. In the final design the repetition rate will be 1.022 MHz.

In the prototype, which operates at 1.9MHz, the electrical pulses that produce this field are stored in a low-loss transmission line. One end of the transmission line is terminated with the open-circuit deflector plates while the other is terminated with a short-circuit (see fig 1). The one way propagation delay from the open-circuit to short-circuit, is about 1μs. A type CY1170J 75kW tetrode [4] whose cathode is at a high negative voltage (-15kV) is utilized to center feed the transmission line. A separate paper at this conference [2] reports on the status of this devices. The complex reflections from the open-circuited and short-circuited ends allow a single tetrode to function both as a charger and as a clipper depending upon the polarity of the reflected pulses. This is illustrated in the lattice diagram (figure 2). A narrow charger pulse, after two reflections, appears at the tetrode with a positive amplitude. By triggering the tube at the trailing edge of this pulse it can be effectively clipped. A second (wide) charger pulse is launched shortly after and is clipped in a similar manner by clip pulse number two (fig 3). When, after five reflections,

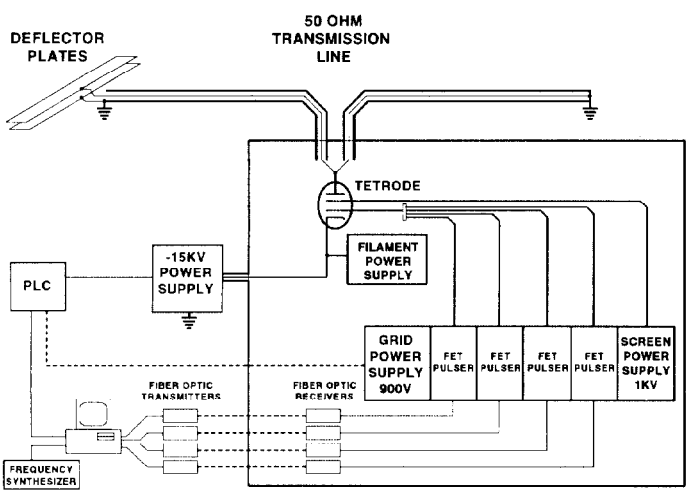

***Figure 1** Beam Chopper*

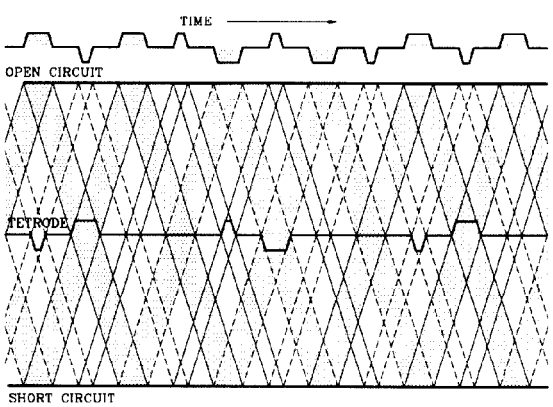

***Figure 2** Lattice Diagram*

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the narrow (or wide) pulses add as a single negative pulse the tetrode is triggered to restore the leading edge.

The quality of the pulse within the center fed transmission line is extremely sensitive to the timing of the grid pulse. A variation of 1ns in the one way cable delay can typically cause a 10-15ns variation in the rise or fall time of the stored pulse. To meet these stringent requirements we built a precision 23MHz grid pulser driven from a synthesizer to simulate the TRIUMF cyclotron main RF.

To drive the tetrode grid, reprogrammable PALs and programmable delay line were used to produce pulse sequences of arbitrary duty cycle and repetition rate. The sequencer output was connected to a FET based grid pulser (fig 1) using fibre optics to give the required high voltage isolation and good noise immunity.

II. HARDWARE

A. Sequencer

The chopper specifications require that alternating narrow (48ns) and wide (92ns) pulses appear at the deflector plates with a repeating pattern corresponding to 45 beam burst [2]. The interval between the narrow and wide pulses must correspond to 20 beam bursts (fig 3). Two programmable logic array devices (PAL16V8) were employed as a counter and state machine to generate the correct sequence of timing and strobe pulses. Clock pulses for the counter are derived from the cyclotron 23Mhz main RF system. Precision programmable delay lines (AD9501) are used to generate pulses of variable pulse width [7]. Each delay line has associated with it two 8-bit latches for pulse width selection (fig 4). An additional delay line provides fine adjustment of the clip pulse timing. Alternating narrow and wide pulses are selected by switching between the two sets of latches (charger widths groups 1 and 2 in fig 4) using strobe pulses generated by the state machine. There are two charger and two clipper channels (A and B). The timing and width of each channel may be independently adjusted to facilitate pulse shape adjustments and to minimize over-swing on the trailing edge of the stored pulse. The pulses are muliplexed and transmitted by four 100Mb/s optical fibre links to the FET pulser units.

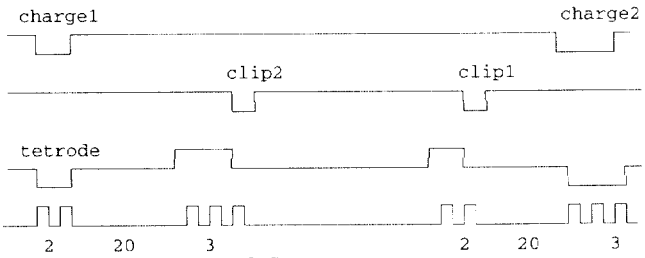

Fig 3 Sequencer output

B. FET Pulser

This device is built around a DEI 150FPS 1kV mosfet driver [3]. It is capable of driving high voltage FETs at frequencies up to 25MHz with pulse widths of 25ns or more with rise times of 3-5 ns. Each channel has two DEI pulser units connected in parallel for a total of eight. The FETs operate

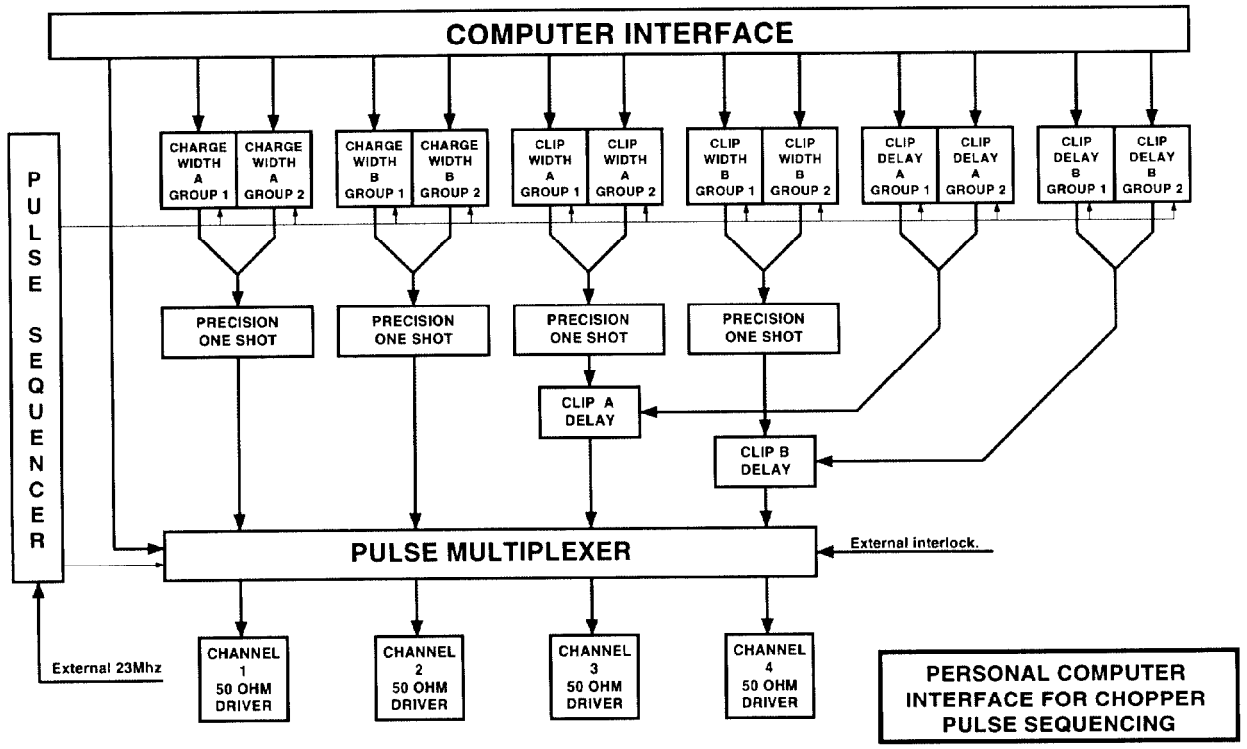

Figure 4 *Block Diagram of the Grid Pulse Sequencer*

with a common but variable source voltage to a maximum of -600 volts. In addition the drain voltage of each of the units can be variable or fixed at ground. Each of the four channels is connected to a summing point close to the grid with one of four 75 ohm coaxial cables. The pulse multiplexer (see fig 4) and the eight FET pulser units allow us to produce a versatile composite grid pulse at the control grid of the tetrode.

An integral part of the chopper test stand is a PC-AT. This is used for a variety of applications including programming the PLC used in the safety interlock system [5]. We therefore integrated the pulser controls by designing the pulser module as a PC card. The PC interface allows the pulse widths and timing to be placed under software control. Also included is a register to monitor the state of an external interlock.

III SOFTWARE

The software is written in the C language and compiled with the Borland C compiler and executes under DOS. Upon startup the pulse widths default to a minimum with all four pulser channels off. A simple user interface (see fig 5) allows the operator to control all pulse width and delay settings. Function keys initiate major system changes and the saving and restoring of settings. The program monitors the state of an external interlock and uses it to disable the pulser if the high voltage power supply is off while the filament is on. This is necessary to protect the screen grid. The status of the pulser and external interlock is displayed on the computer screen.

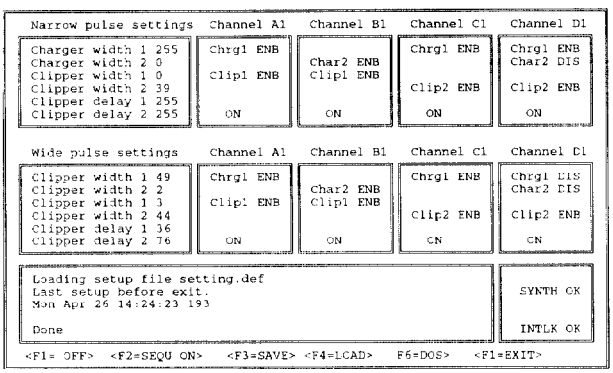

***Fig 5** Pulser Control Screen*

IV FUTURE DEVELOPMENT

A. Pulser

The current mode of operation is open loop thus we have no control over long term drift. A timing shift relative to a master trigger is not a major concern since in a sense the chopper is the master trigger for KAON. However, as already described, drift in the clipper timing can have a major effect on the shape of the chopper pulse. This can manifest itself as a change in the DC level of the inter-pulse region. We plan to add a gated ADC to detect this level and use the signal to adjust the settings. In the final design we may need to double the number of parallel FET pulsers and the number of clip delays in order to improve the control of the inter-pulse ripple.

B. Computer

Although adequate in a development environment a PC does not represent a good choice for an operational system. We are currently developing an intelligent controller for applications in embedded systems. The controller is a single-board module in a Euro-card format based on a Motorola MC68332 microcontroller. An onboard Ethernet interface will allow software downloading and remote device control. Also included are 8 A-D channels, 8 D-A channels, 48 bits of digital I/O and 2 serial ports. The controller is designed to function as a VME slave device. Enough EPROM capacity will be included to hold large standalone application software including the VxWorks kernel [7]. We plan to redesign the pulser module as an expansion board to this controller.

V REFERENCES

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