

# Frequency Control of RF Booster Cavity in TRIUMF

K. FONG and M. LAVERTY

TRIUMF, 4004 Wesbrook Mall, Vancouver, B.C., Canada, V6T 2A3

## Abstract

A booster cavity is used in the TRIUMF cyclotron to increase the energy gain per turn for beam orbits corresponding to energies greater than 370 MeV. It operates at 92.24 MHz, the 4<sup>th</sup> harmonic of the cyclotron main rf, and at a nominal voltage of 150 kV. Excitation is provided by a 90 kW rf system that is phase locked to the main rf. When the main rf is interrupted due to sparking or other causes, a controller built into the low level frequency source of the booster rf system disables the phase-locked loop, and reconfigures the source as a temperature stabilized oscillator operating at the last locked frequency. When the cyclotron rf is restored it usually will be at a different frequency. The oscillator tunes automatically to this new frequency. The acquisition time is extended by the controller to match the response time of the mechanical tuner in the cavity.

## I. INTRODUCTION

The TRIUMF rf booster is an auxiliary accelerating cavity operating at the 4<sup>th</sup> harmonic of the cyclotron rf. It provides 150 kV at its accelerating gaps for additional acceleration of the beam at energies above 370 MeV [1], [2]. By altering the phasing between the fundamental and the 4<sup>th</sup> harmonic one can also produce longitudinal splitting of beam bunches [3]. There are several requirements that the frequency source for the rf booster must satisfy. First, for proper acceleration of the beam the 92.24 MHz booster rf must be phase-locked to the 23.06 MHz cyclotron rf at the dee. This is necessary since the cyclotron rf is not phase regulated, and its phase varies as the resonator detunes due to mechanical vibrations. Second, when using the cyclotron rf as the reference, it is liable to shut off due to a variety of reasons. When this occurs it is desirable to maintain rf power in the booster for thermal stability reasons. Third, when the reference returns after a length of time, it will usually be at a different frequency. The source cannot jump instantly to this new frequency since the booster cavity is not tuned to this new operating point. The transition must be gradual enough for the mechanical tuning system to follow. Fourth, the frequency source should be capable of being decoupled from the reference and performing limited frequency sweep. This is necessary during power up sequencing for cavity conditioning. The above requirements are met with a multiply by 4 phase-locked loop that is able to work with the non-cooperative cyclotron rf as the reference. A digital sample and hold circuit driving the voltage controlled oscillator in the PLL enables the oscillator to free run at the

same frequency when the reference is absent, for intervals from minutes to hours. An embedded microcontroller controlling the S/H circuit is used to extend the acquisition time of the phase-locked loop when the cyclotron rf is restored at a different frequency. The input to the VCO is only permitted to vary slowly under software control. Furthermore, this control also allows one to sweep the output to find the most favorable frequency during power-up sequencing.

## II. SCHEMATIC DESCRIPTION

A functional block diagram of the frequency source is given in Figure 1. Its main components consist of a multiply by 4 analog phase-locked loop with an input frequency of 23.06 MHz, and a pair of Analog-to-digital/Digital-to-analog converters controlled by a microcontroller. During normal

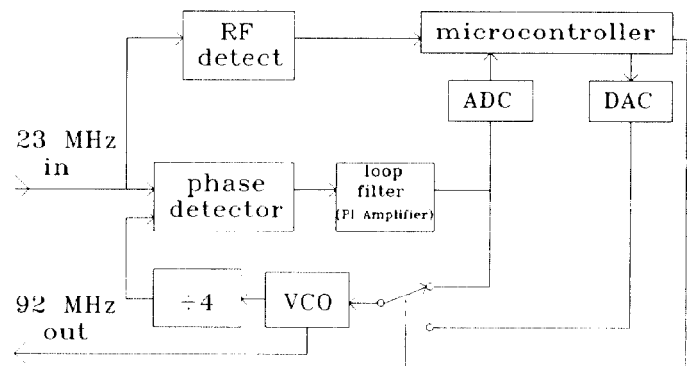


Figure 1. Over-simplified Functional Block Diagram of the booster frequency source.

operation, when the input reference is present, the PLL operates as a second order loop. A frequency/phase detector compares the phases between the reference input from the cyclotron rf and a divided by 4 output of a VCO with a centre frequency of 92.24 MHz. The phase difference is filtered to remove the 23 MHz component. It is connected by an analog switch to the loop filter, a proportional-integral amplifier, whose output is used to vary the frequency of the VCO. This results in a second order feedback loop, with one integration provided by the loop filter and the other provided by the VCO. The microcontroller assumes a supervisory mode and instructs the ADC to repetitively sample the voltage at the loop filter output. This value is stored in the memory of the microcontroller. When the reference is off, the microcontroller breaks the feedback path and reconfigures the source to operate in an open loop mode. It recalls the stored value of the last sampled voltage, converts it into analog

voltage via the DAC and drives the VCO to the last sampled frequency. The switching between the loop filter output and the DAC output is designed to prevent voltage spikes from appearing at the VCO input. Due to its very high low frequency gain, the PI amplifier once taken out of the feedback path will have integrator wind-up, and cannot be switched in again without causing a voltage spike. For this reason the PI amplifier is always in some sort of feedback path. During open loop operation, the PI amplifier is incorporated in a minor loop as shown in Figure 2. The output of the DAC does not drive the VCO directly, but instead is compared with the output of the PI amplifier and the error is feedback to the input of the PI amplifier. This completes a voltage feedback loop that regulates the output of PI amplifier to be the same as the output of the DAC. The output of the PI amplifier is at all times connected to the VCO. When the reference is restored, the microcontroller measures the frequency differences between the input and the VCO output/4, and instructs the DAC to slowly ramp the VCO towards the 4<sup>th</sup> harmonic of the input. This slow ramping is necessary since, if the difference in frequency is large when compared to the resonator bandwidth, simply

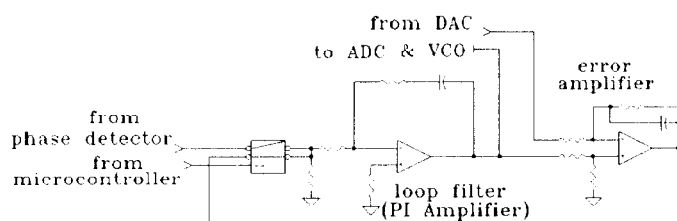


Figure 2. Detailed schematic of minor loop between the loop filter and the phase detector for glitchless closing of PLL.

enabling the PLL will cause a fast frequency shift and the mechanical tuning motors would not be able to catch up. This would result in excessive forward and reverse power demands from the power amplifier and can cause catastrophic failure of the power amplifier. When the microcontroller detects that the difference in frequency is less than the 3 dB bandwidth of the cavity, the switches are re-engaged to enable normal closed loop operation. The DAC is also stepped during the initial power up sequencing. By sweeping the frequency this way one is able to choose the optimum frequency for cavity conditioning.

### III. BANDWIDTH

Measurements show that the phase detector gain  $K_\phi$  is 0.16V/rad and the VCO gain  $K_o$  is  $8.3 \times 10^5$  rad/sV. The closed loop gain of a  $\times 4$  PLL with a PI loop filter having proportional gain  $A_p$  and a zero at frequency  $\omega_b$  is given by [4]

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2},$$

where  $\omega_n = 1/2 \sqrt{K_f K_\phi \omega_b A_p} = 1.82 \times 10^2 \sqrt{\omega_b A_p}$  is the closed loop bandwidth, and  $\zeta = \omega_n / 2\omega_b = 9.1 \times 10^1 \sqrt{A_p / \omega_b}$

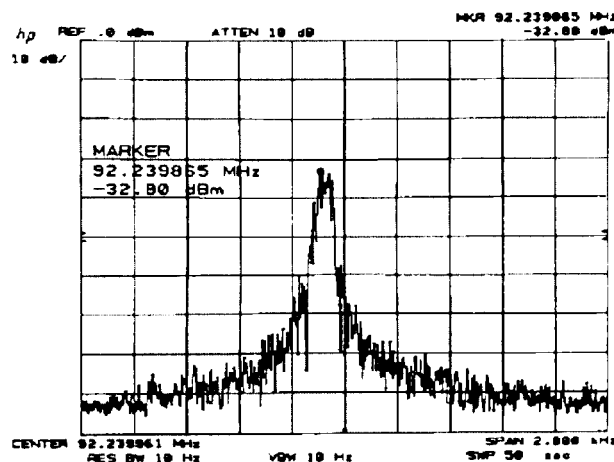


Figure 3(a). Spectrum of VCO output in unlocked condition

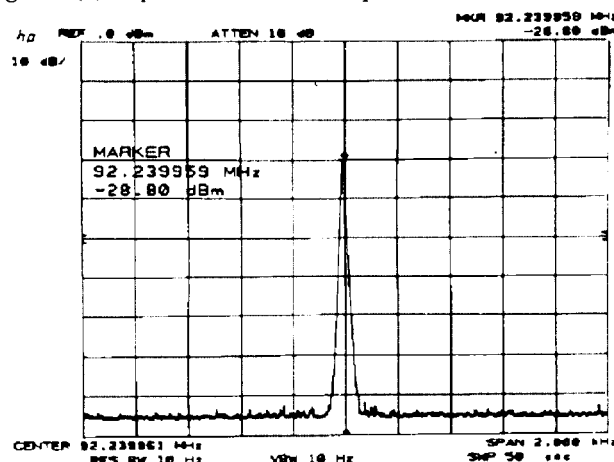


Figure 3(b). Spectrum of VCO output in locked condition

is the damping factor. The design starts with a target bandwidth of 500 Hz and a damping factor of 2. Using standard component values one gets a bandwidth of 425 Hz and a damping factor of 1.7. The open loop gain at 5 Hz is 10,000. Since the phase variation of the reference is predominantly due to mechanical vibrations of the resonator structure that centers at 5 Hz, this open loop gain is more than sufficient to track the phase variation occurring in the reference.

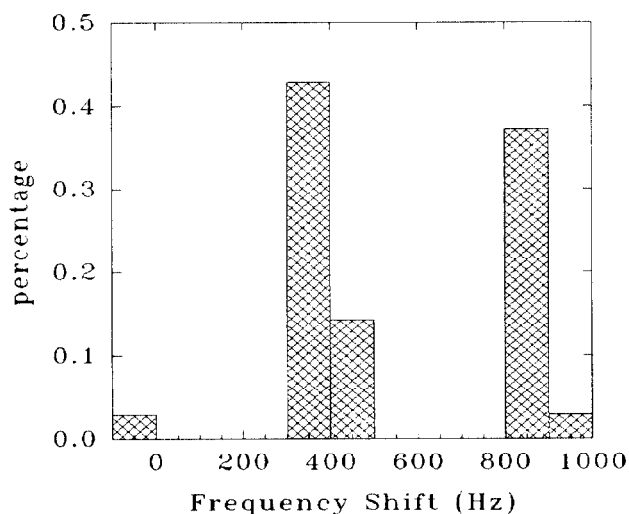


Figure 4. Amount of frequency shift when the frequency source switches from phase locked mode to free running mode.

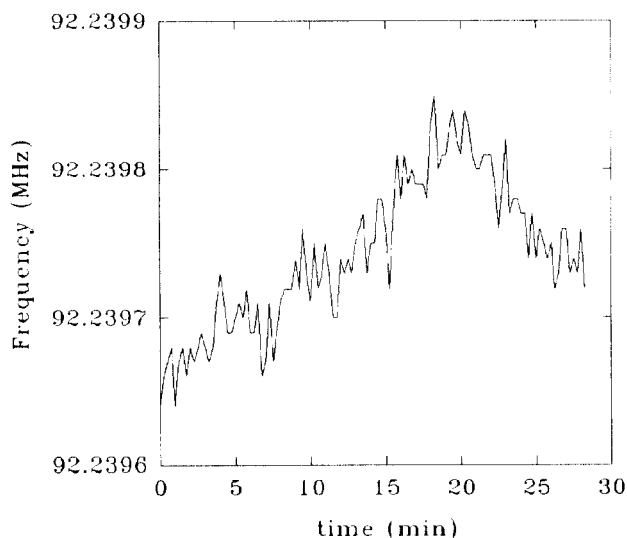


Figure 5. Frequency variation of the VCO in free running condition.

Since the acquisition process is controlled by the microcontroller, with the DAC driving the VCO, the capture range of the frequency source is determined by the voltage swing capability of the DAC. With an 8-bit DAC, the frequency step in turn is 1/256 of the capture range. This leads us to a compromise of a 400 Hz step size, resulting in a 100 kHz capture range. This gives sufficient range to lock on to the main cyclotron rf during warm-up and normal operating conditions.

## IV. SPECTRAL OUTPUT

Comparison of the output spectra of the source under locked and unlocked condition is shown in Figure 3. The actual output power is +13 dBm but is attenuated at the input of the spectrum analyzer. Figure 3(a) shows the output when the PLL is disabled. Frequency stability and phase noises are not particularly good. This is to be expected from a free running VCO. The output spectrum improved significantly when the PLL is enabled and locked as shown in Figure 3(b). In this case spurious noises are at least 55 dB below carrier. Fig. 4 shows the statistical distribution of the frequency shift at the output of the PLL when the input reference is switched off. Due to digital quantization there are 3 distinct peaks of shift, each separated by about 400 Hz, which is in agreement with the selected step size. One can also see that the maximum shift is less than 1 kHz, well below the bandwidth of the cavity. The "long" term frequency stability under free running condition is shown in Figure 5. The maximum frequency excursion is only 200 Hz over a time interval of 30 minutes. This stability is obtained by using temperature compensating capacitors in the VCO LC tank circuit.

## V. CONCLUSION

The performance of the frequency source of the booster has to satisfy several requirements: it must be able to track the phase and frequency variation of the reference input, which may be absent for a long period of time, while acquisition time must be slow enough for the mechanical tuning system to follow. These would be conflicting requirements in an ordinary PLL, but are avoided by using an embedded microcontroller to control the operation of the loop. This controller determines the acquisition timing, as well as the opening and closing of the analog PLL. Safe and reliable operation of the source has been demonstrated with this system.

## VI. REFERENCES

- [1] R.E. Laxdal, K. Fong, G.H. Mackenzie, V. Pacak, J.B. Pearson, L. Root, M. Zach, "Initial Operating Experience with the Auxiliary Accelerating Cavity for the TRIUMF Cyclotron," IEEE Particle Accelerator Conference Proceedings, San Francisco, May 1991, pp. 810-812.
- [2] K. Fong and M. Lavery, "RF Control for TRIUMF Booster Cavity," Proceedings of the Third European Particle Accelerator Conference, Berlin, March 1992, pp. 1176-1178.
- [3] R.E. Laxdal and W. Joho, "Longitudinal Splitting of Bunches in a Cyclotron by Superposition of Different RF Harmonics," Proceedings of the Third European Particle Accelerator Conference, Berlin, March 1992, pp. 590-592.
- [4] R.E. Best, "Phase-Locked Loops," McGraw-Hill, 1984.