NANOSECOND MOSFET GUN PULSER FOR THE CESR HIGH INTENSITY LINAC INJECTOR

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Abstract

A fast solid-state pulser (PFH) for the Cornell CESR linac injector system is described. Stripline-packaged high-voltage power MOSFET devices are arranged in a novel cascode output topology to achieve extremely low transition times. In the present CESR injector, the PFH driver outputs pulses of 3 nanoseconds FWHM and 20 amperes peak current through an Eimac Y-796 cathode-grid assembly. Recovery time is approximately 10 nsec. Advantages of the MOSFET pulser over its hard-tube predecessor include a substantial increase in peak beam current, an order-of-magnitude reduction of gun interpulse recovery time and precise control of the unequal output pulse amplitudes required for e^+ vs e^- injection modes. Reduction of physical size permits collocating the pulser with the linac electron gun assembly to minimize transmission line artifacts arising from unavoidable impedance mismatch over the gun's bias range. Successful implementation of the MOSFET linac gun pulser is an initial step to a future CESR B-factory injector.

Introduction

Injection rate into the CESR storage ring strongly affects collider integrated luminosity, principally due to time lost during replenishment of the beams. Upgrades of the CESR injector's gun, linac and synchrotron over the past decade have thus far yielded more than an order of magnitude improvement in average charge transport during fill periods. A significant step forward has been achieved by replacing the previous linac hard-tube gun pulser with a solid-state module of markedly superior performance. Cornell has recently begun investigating multibunch train operation as an avenue to higher luminosity, and the MOSFET linac gun pulser described here (Figure 1) is an essential component of that program.

Key parameters for a CESR multibunch-train compatible injector gun driver are: peak pulse current of 20 amperes, pulse FWHM 3-5 nanoseconds, maximum repetition rate 72 MHz and recovery time less than 12 nanoseconds. Although

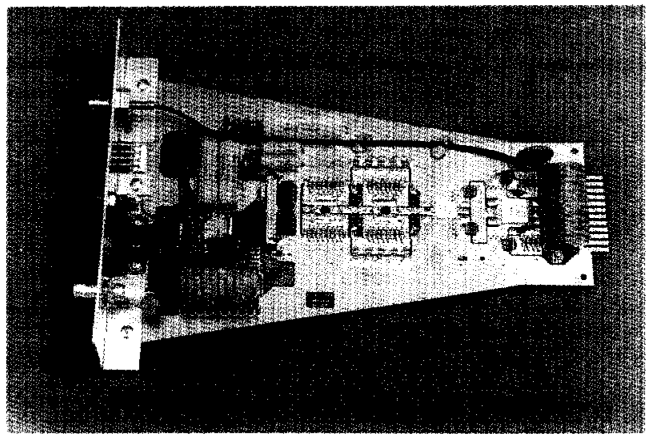

Figure 1. Nanosecond gun pulser assembly.

solid-state pulsers exist in many forms, including the familiar avalanche bipolar and step recovery types, output capabilities of these and other fast pulser solutions are either inadequate or the technologies are too costly for CESR injector use. Several years ago, preliminary work at Cornell using SPICE simulations and breadboard measurements indicated a power MOSFET cascode output topology could meet specifications at reasonable cost, if and when r.f.-packaged H.V. pulse power MOSFET devices became available.

Eventually, commercial r.f.-packaged high-voltage, high pulse power MOSFET's were located, and a stripline pulser breadboard utilizing the devices was then assembled. With specific MOSFET parameters in hand, SPICE modeling proved useful for successfully "fine tuning" the cascode design. Performance of the prototype met expectations for peak output and pulse width, the only shortfall being a longer than expected recovery interval. The longer recovery time did not affect contemporary 7 bunch CESR operations, so a MK I version of the MOSFET gun pulser was installed in the Cornell High Intensity Linac Injector[1] (CHILI) in mid-1991.

After approximately one year of service, the pulser (and spares) were upgraded in preparation for CESR multibunch-train studies. A troublesome energy storage mechanism was found to exist in the intermediate driver stages. By substituting custom stripline packages for the earlier

♦ Work supported by NSF grant PHY-9014664.

paralleled DIP arrays in these stages, recovery time constant and pulse to pulse crosstalk were reduced to a negligible level.

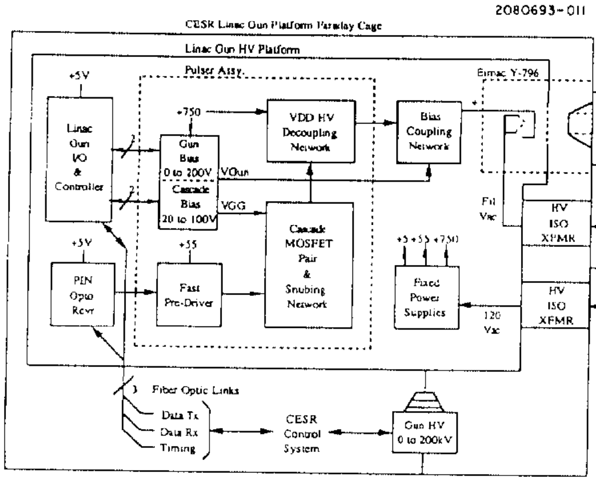

Figure 2. CESR CHILI injector HV platform.

CHILI systems

A block diagram of linac gun support systems is presented in Figure 2 with MOSFET pulser circuit board subsystems shown in the dashed area. Peripherals in the gun tank include fixed power supplies and I/O controller. The nanosecond pulser is mounted in the high-voltage tank approximately two centimeters from the EIMAC cathode assembly to minimize transmission line artifacts which can degrade pulse to pulse isolation. Timing signals are sent to the pulser over a fast (tr, tf ≈ 2.5 nanoseconds) fiber optic link. Control data sent over a lower bandwidth CESR control system optical link determine the level of the V_{GUN} and V_{GG} bias supplies associated with the gun pulser. Upstream serial information includes readback of all supply voltages and the detected pulser output level.

Pulser design

A simplified schematic of the nanosecond gun pulser is shown in Figure 3. Fast response in all stages is obtained by avoiding operation in or near the MOSFET devices' depletion-transition region. This is accomplished by maintaining $|V_{DS}| - |V_{GS}| > 5$ volts under worst-case conditions (e.g., when the cascode pair is biased for minimum pulse amplitude). All critical MOSFET signal paths are controlled-impedance striplines within the multilayer circuit board.

Predriver and drivers consist of a paralleled array of 74ACT-series high-current gates followed by two discrete stages, shown in Figure 4, which provide level conversion and additional power gain. Both stages consist of a single MOSFET die bonded to a small circuit board which serves as a stripline substrate, as seen in Figure 4. The technique is known as chip-on-board, or COB, fabrication[2] and is a cost-effective r.f. construction method.

Output devices DE101N05 and DE102N05 are stripline-packaged, commercially available[3] power MOSFET's. The input (lower) device is selected for small input C_{iss} and relatively low R_{Don}, while the output (upper) device is specified for high (1 KV) V_{DS} capability. Both devices exhibit good r.f. characteristics to the 400 MHz region. By arranging the output devices in a cascode topology to minimize Miller-effect loading, charge gain remains high and the inherent device bandwidth is retained. The cascode arrangement also permits wide-range adjustment of output amplitude via programmable bias voltage source, V_{GG}, applied to the DE102N05 gate. Details of the output section, including the output H.V. decoupling network, are displayed in Figure 5.

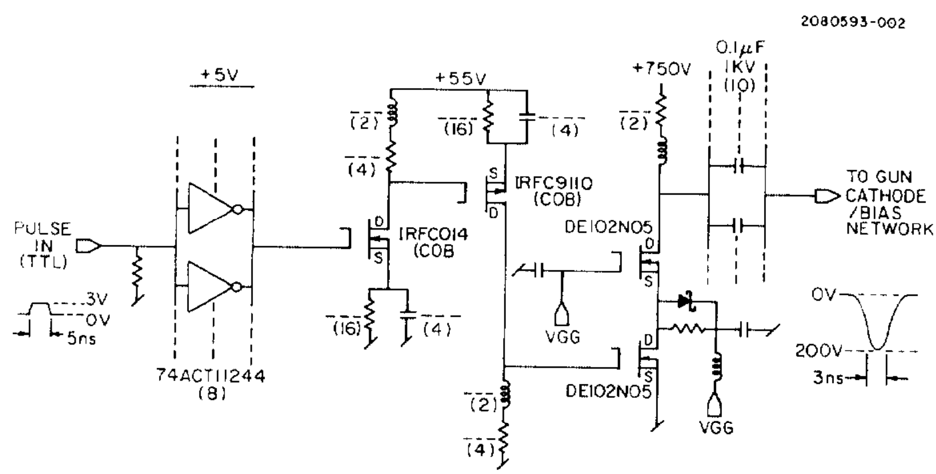

Figure 3. Driver and output schematic.

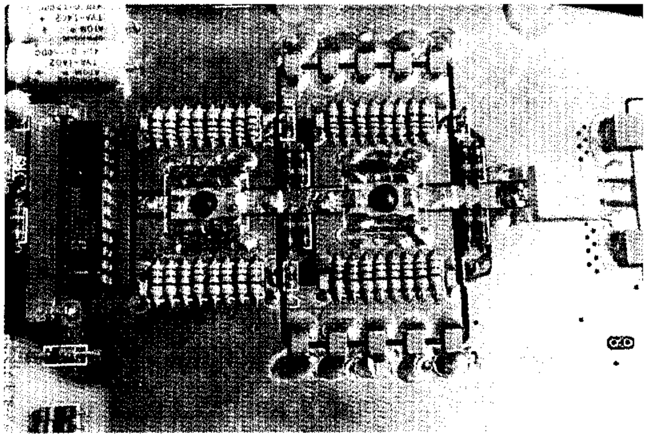

Figure 4. Intermediate driver stage detail.

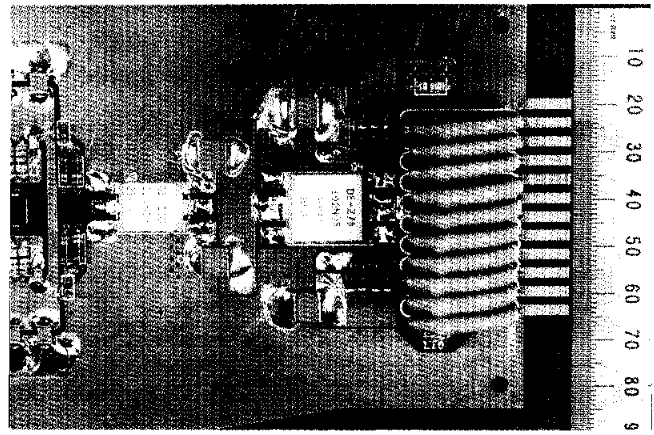

Figure 5. Pulser output and coupling network detail

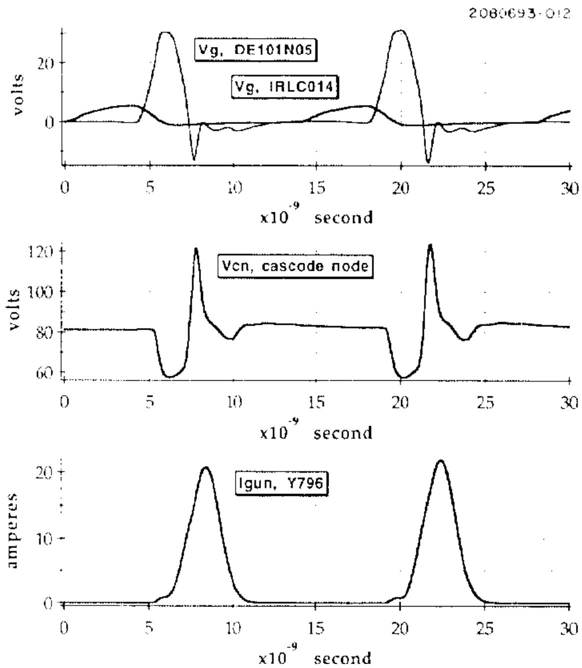

Figure 6. Pulser waveforms under e^+ injection conditions.

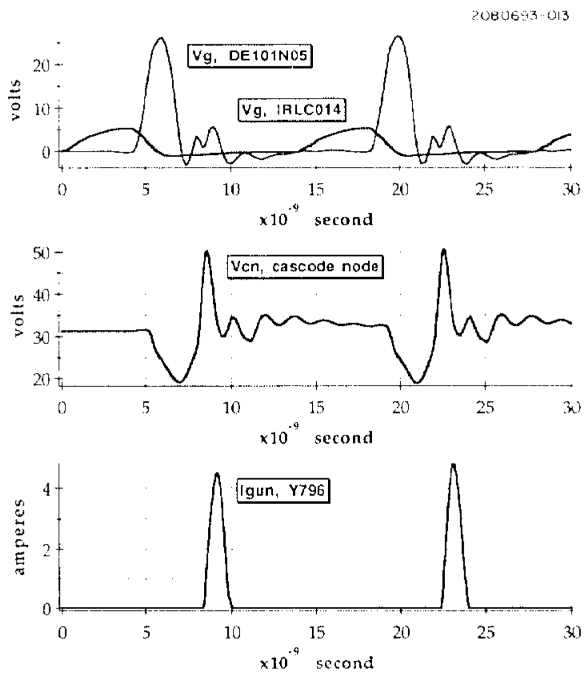

Figure 7. Pulser waveforms under e^- injection conditions

Performance

Measurements of electron bunch charge exiting the gun assembly under varying bias conditions are in good agreement with SPICE predictions, as revealed by bench observations of the cascode node and output waveforms. We find that level 3 MOSFET modeling provides correspondence within a few percent of observed fast pulser characteristics. Simulation waveforms of Figure 6 (e^+) and Figure 7 (e^-) accurately depict pulser behavior over an order of magnitude programmed output range (injection intensity is attenuated during CESR electron filling to avoid space charge induced loss through the linac pre-bunchers and excess radiation). For both waveform sets, a noteworthy feature is the relatively small variation in output pulse amplitude evident in comparison of the first gun current pulse to subsequent 14 nanosecond-spaced pulses.

Conclusions

We have found, for present and projected CESR injection parameters, the stripline-MOSFET solid state pulser provides superior performance when compared with hard-tube or other solid-state alternatives. A MK II version of the CESR MOSFET "Pulser from Hell" is presently operational in the CESR injector and meets critical parameters for B-factory-compatible 14 nanosecond CESR multibunch-train injection.

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[1] E.B. Blum et al, "Performance of the Cornell High Intensity Linac Injector", LNS CBN 83-8, 1983

[2] Argo Transdata Corp., Clinton, CT, 203-669-2233

[3] DEI, Inc., Fort Collins, CO, 303-493-1901