

## FAST THYRATRON DRIVER\*

M. N. NGUYEN AND R. L. CASSEL

Stanford Linear Accelerator Center  
Stanford University, Stanford, California 94309

### Abstract

A fast solid-state pulse generator used as a thyatron grid driver for kicker pulsers, has been developed and built with power MOSFETs and a transmission line transformer. The MOSFET, pulsed on and off by a pair of P-N channel HEXFETs, switches charged capacitors into the transformer connected in parallel on one end and in series on the other end to step up the voltage. The resulting output pulse parameters are 2 kilovolts peak (into 50 Ohms), 13 nanoseconds risetime (10-90%), 250 nanoseconds duration, and less than 50 picoseconds pulse-to-pulse jitter. Various methods are employed to protect the MOSFETs from thyatron arc back, including the use of TransZorbs and a magnetic diode.

### Introduction

For improved performance of kicker systems, the stability and reliability of thyatron grid drivers play an important role. Earlier drivers at SLAC used SCRs as switching devices in resonant charging circuits and, although they worked well for many years, produced output pulses with slow rate of voltage rise and long throughput delay which contributed to high jitter and extended delay time of the main thyatron current. Experiments have shown that a high amplitude, low impedance and fast rise grid trigger pulse could reduce anode current time jitters.

This led to the development of a new thyatron grid driver. The circuit basically is an RC pulse generator where capacitors are charged over a long period of time and then discharged rapidly through a step-up transmission line transformer to produce an output pulse with a fast risetime and multiplied amplitude. Using a transmission line, with its frequency-independent characteristic impedance, as a transformer lead gives a high degree of coupling and virtually no delay between the transformer primary and secondary. Power MOSFETs are chosen as switching devices because they are inherently fast and the gate drive circuit is relatively simple and requires minimum drive power.

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### Design

A simplified schematic diagram is shown in Figure 1. The circuit consists of six identical power MOSFET switches and gate drivers, a transmission line transformer T1 and a magnetic diode X1. Only one switch and its gate drive is drawn for simplicity. The MOSFET gate driver is based on Directed Energy switching test circuit with front end (not shown) added to accommodate various interlocks and signal indicators. A TTL trigger provides input voltage for the Clock Driver DS0026 to drive the complementary P-N channel HEXFETs, IRFD9120 and IRFD110, which in turn generate the pull up and pull down for the power MOSFET gate. R1 and R2 serve to limit the HEXFETs drain voltage spike. R3 terminates Q3 gate to prevent the device from turning on in an open circuit while D1 protects it from over voltage.

The transmission line transformer consists of six strip transmission lines, each having an equal length of 24 inches and a characteristic impedance ( $Z_0$ ) of about 10 Ohms, which wound around a ferrite core (Ceramic Magnetics CMD 5005). There is one turn on the first line, two turns on the second line and so forth, six turns on the sixth line. Each line in essence is a unity-coupling transformer with different impedance. One side of each line primary and secondary are then driven in parallel by charged capacitors while the other side cascaded in series with the load. The net result is that of a conventional transformer with a step-up voltage ratio of six to one and an extremely wide bandwidth. The transformer has an input impedance of:  $Z_p = Z_0 / 6 = 1.7$  Ohms, and an output impedance of:  $Z_s = Z_p \times N^2 = 1.7 \times 6^2 = 60$  Ohms. The low-frequency cutoff is determined by:  $f_l = X_L / 2 \times \pi \times L$ , where  $X_L = Z_0$  and  $L = 0.4 \times \pi \times N^2 \times \mu \times A_c \times 10^{-8} / l$ . For  $N = 1$ ,  $\mu = 2500$ ,  $A_c = 2.58$  cm<sup>2</sup>, and  $l = 11.97$  cm, the low-frequency response is about 235 kilohertz. With given length of the line, the high-frequency cutoff predicted at one-eighth of wavelength in free space is:  $f_h = 0.125 \times v / l = 61$  megahertz.

Let's consider circuit operation on the first line. A 400 volts power supply charges capacitor C2 to full voltage over time. When Q3 is turned on, C2 discharges quickly through C3, D6 and the strip line producing magnetic flux at the core and a negative voltage signal at the transformer primary. The

signal, when propagating through the length of the line, induces an equal and opposite voltage at the transformer secondary where its negative end is bypassed to ground through C3. The induced positive end ( $V_{IND}$ ) summed up with charged negative voltage apply twice the voltage across the second line with its two turns to match the impedance. Thus, the second line induced voltage now is twice the power supply voltage.

As it can be seen, the remaining four lines react in a similar manner. The sixth line finally induces a voltage that is six times the power supply voltage with a load current equals to all capacitive discharging currents. All capacitors in effect combine in parallel to provide power to the load. Moreover, the power supply negative side is floating to provide a 30 Volts negative bias voltage to the thyatron grid.

#### Performance

Figure 2 shows the output waveform measured into 50 Ohms resistive load. The voltage quickly rises to 2 kilovolts peak, then slowly decays with a  $Z_0C$  time constant of 0.5 microseconds where the tail collapses because of transformer core saturation. As seen, instead of six to one, the voltage ratio is closer to 5.4:1, ten percent less than the perfect condition. This loss is incurred by series impedances associated with power MOSFETs  $R_{DS(on)}$  and capacitors ESR which resulted in reducing the line charging voltage. Pulse width at half maximum (FWHM) is about 250 nanoseconds. A larger value of charge capacitors will generate a wider pulse. Since the transformer retains transmission line characteristics, the output risetime is mainly determined by the switching times of power MOSFETs and gate drivers. A risetime of 13 nanoseconds, 10 to 90 percent, is shown in Figure 3. The MOSFETs used were DE-275 501N12 from Directed Energy Inc. This device is rated at 96 Amps peak, repetitive pulses, and has a voltage rating of 500 Volts.

Throughput delay, defined as the sum of the total turn-on and the propagation delay times of each device in the signal path, is less than 100 nanoseconds.

Jitter and drift as measured with an SR620 Universal Time Interval Counter showed excellent performance. The test, conducted with a sample size of ten thousand shots and 120 Hertz repetition rate, displayed a peak-to-peak jitter of less than 300 picoseconds with a standard deviation or rms jitter of less than 50 picoseconds.

Protecting the MOSFETs from failure due to drain-to-source breakdown proved to be an interesting task. High transient voltages of many kilovolts combined with low source impedance returning from the thyatron grid posed great risk for the device. Furthermore, transient pulse width may also vary from ten to hundreds of nanoseconds depending on the type of thyatron breakdown. These fault conditions justified a redundant MOSFET protection scheme. Referring to Figure 1, presume that a positive kick-back transient traveled through the transformer, fast recovery diode D4 turns on to clamp the voltage down. If there still is current flowing toward the MOSFET drain, snubber circuit R4-C1 along with effective series inductances reduce  $dv/dt$  and the peak transient voltage while D2 clamps the potential to the power supply voltage level. The same case applies to negative kick-back transients where D3 now provides clamping action.

Limiting transient voltages at the transformer output are TransZorbs, General Semiconductor 1.5KE200. These high peak power dissipation, extremely fast response suppressors theoretically can clamp transient voltages in less than one picosecond. However, twelve devices are needed for 2400 Volts breakdown voltage and lead inductances are in series. It results in an increase of response time to about 20 nanoseconds.

The first and probably most effective defence against the returned transients is the so-called 'magnetic diode'. As its name implies, the device can pass a large forward current while blocking it in the reverse direction by means of a saturable magnetic core. It is a transformer with one turn on the secondary and nine turns with large inductive and capacitive coupling on the primary side, wound around a high frequency ferrite core (CMD5005). A DC current applied on the primary forces the core into positive saturation. The saturated inductance impressed on the secondary is so small that it opposes little to the forward pulsed current. In the reverse direction, magnetizing inductance grows considerably to limit the transient current flow. Diode breakdown, or the ability of the transformer to stop transient current from flowing back, is determined by the Volt-second product, which is:  $E \times t = 2 \times N \times B_m \times A_c \times 10^{-8}$ . Where  $N = 1$ ,  $B_m = 3300$  Gausses,  $A_c = 1.29 \text{ cm}^2$ , the Volt-second product is 85 kilovolts nanosecond. The applied forward bias current is about 3 Amps, determined by:  $I = H \times l / 0.4 \times \pi \times N$ , where  $H$  (from the core data sheet) = 10 Oers,  $l = 3.19 \text{ cm}$ , and  $N = 9$ .

Conclusions

References

The development of this project has produced a fast voltage rise and extremely low jitter triggering source for thyratrons. Its high performance is contributing to the reliability and stability of kicker magnet systems at SLAC.

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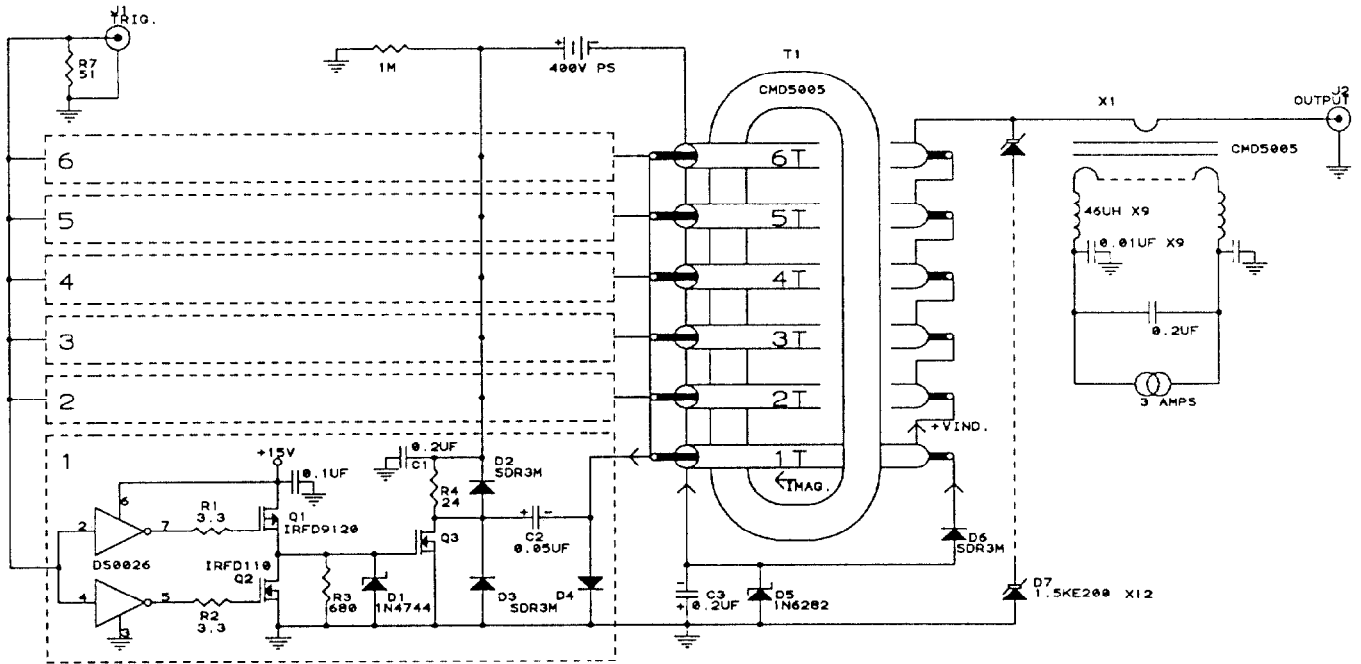


Figure 1. Simplified Schematic Diagram.

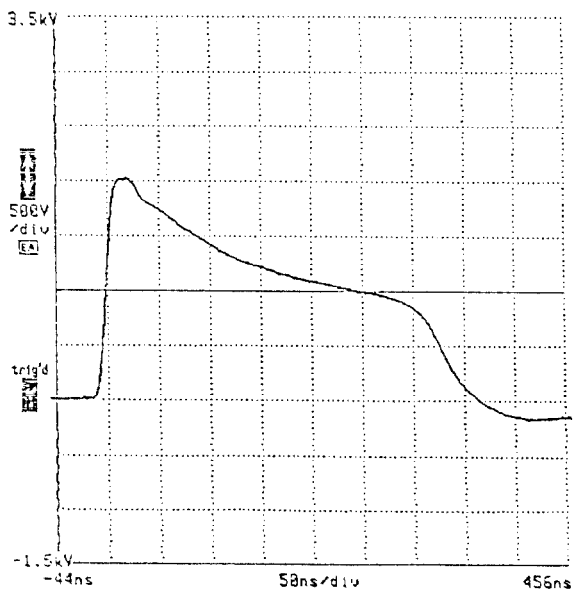


Figure 2. Output Waveform. 50 Ohms Load.

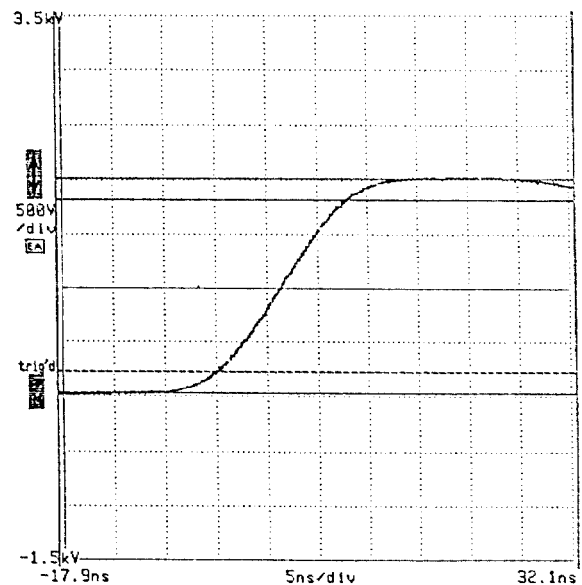


Figure 3. Voltage Rise.